VTK DESIGN SEMINAR 2026

일 시 : 2026년 10월 22일(목요일) 09:30~17:30
장 소 : 양재 엘타워 5F, 오르체홀

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AGENDA / 2026.10.22 THU

VTK DESIGN SEMINAR 2026

Cadence AI부터 회로 · PCB 설계, SI/PI · 3D Simulation까지.
앞으로 바뀔 설계 환경을 하루에 살펴봅니다.

DATE	TIME	VENUE	ENTRY
2026.10.22 목요일	09:30 ~ 17:30 09:30 등록 시작	양재 엘타워 5F 오르체홀	무료 사전등록제 · 150석

01 / MORNING 09:30 ~ 12:00

올해 무엇이 바뀌었는지

09:30 ~ 10:00	REGISTRATION		
10:00 ~ 10:10	Welcome Speech	Verity Technology Korea	김준한
10:10 ~ 10:30	What's New in OrCAD X Capture	Verity Technology Korea	이정희
10:30 ~ 11:00	Design Analyses in Allegro X System Capture & What's New	Verity Technology Korea	전현우
11:00 ~ 11:30	PSpice What's New & Key Feature Highlights	Verity Technology Korea	공연희
11:30 ~ 12:00	What's New in Allegro X PCB Editor & IC Packaging	Verity Technology Korea	박예솔
12:00 ~ 13:30	LUNCH TIME		

02 / AFTERNOON 13:30 ~ 17:30

어디로 가고 있는지

13:30 ~ 14:00	Cadence SDA 솔루션을 통한 AI기반 통합 시스템 설계 및 다중물리 해석	Cadence Korea	도지훈
14:00 ~ 14:30	AuraStack AI Super Agent : From Engineering Intent to Implementation	Cadence Korea	오영주
14:30 ~ 15:10	BREAK TIME		
15:10 ~ 15:40	Clarity / Sigrity Technologies : What's New & Roadmap	Cadence Korea	김성주
15:40 ~ 16:10	PLM 기반 OrCAD Capture CIS Interface 구축 사례	HL Klemove	이수열
16:10 ~ 16:30	Integrity System Planner를 활용한 Package Connectivity Check & Verification	HANA Micron	김수정
16:30 ~ 17:00	Next-Generation 3D-IC Design and Verification Platform	Verity Technology Korea	박용진
17:00 ~ 17:30	기념품 증정 현장 설문에 참여해 주신 분께 드립니다		

* 상기 발표 순서 및 내용은 사정에 따라 변경될 수 있습니다.

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(13595) 경기 성남시 분당구 황새울로200번길 36 분당 동부루트빌딩 11층
TEL 02-2057-8815 · verity@veritytech.co.kr · www.veritytech.co.kr

What's New in OrCAD_X_Capture

이 정 희
(Verity Technology Korea)



26.1 : 25.1 Base ~ HF050에서 추가된 기능을 모두 포함

26.1 What's New의 주요 기능은 모두 25.1 Base, Hotfix에서 처음 도입된 기능

기능	최초 도입	슬라이드
PDF Export간소화	25.1 HF050	16
TI 모델 라이브러리 접근 (Component Explorer)	25.1 HF040	14~15
회로도 Design Review · Markup	25.1 Base	6
Advanced Find and Replace Properties	25.1 Base	7~10
Design Template 저장 · 불러오기 (.dtp)	25.1 Base	11
OnCloud 라이선스 여러 기기 사용 (최대 5대, Borrow)	25.1 Base	12

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발표 순서

25.1 Base ~ HF050 기능 중심으로 소개

1. **Hotfix 릴리스 일정**
   25.1 Base ~ HF050
2. **25.1 Base 신규 기능**
   Design Review, Advanced Find and Replace, Design Template
3. **라이선스 변경**
   OnCloud 라이선스 다중 기기 설치, Borrow
4. **Hotfix 신규 기능**
   TI Model Libraries (HF040), PDF Export (HF050)

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25.1 Base 이후 Hotfix 일정

Capture 신규 기능은 HF040, HF050에서 추가

릴리스	릴리스 날짜	Capture 신규 기능
25.1 Base	-	Design Review, Advanced Find and Replace, Design Template, 라이선스 변경
HF010	2025-12-12	없음
HF020	2026-02-12	없음
HF030	2026-04-10	없음
HF040	**2026-06-18**	**TI Model Libraries**
HF050	**2026-07-31**	**PDF Export 간소화**

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What's New in OrCAD X Capture V25.1

25.1 Base 신규 기능과 변경 사항

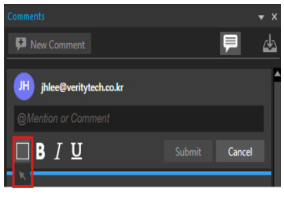
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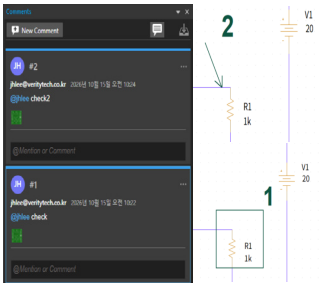
Design Review and Markup

Capture에서 코멘트와 마크업으로 회로도 검토

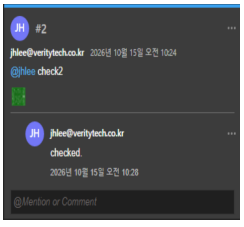
- **실행** : Tools > Markup
- **코멘트 작성** : New Comment > 코멘트 입력, @로 사용자 태그 > Submit
- **마크업** : 코멘트 카드에서 마크업 모양(사각형, 화살표) 선택 후 캔버스에 영역 표시
- **답변** : 같은 스레드에 답변



마크업 모양 선택



코멘트 #1, #2와 회로도 마크업



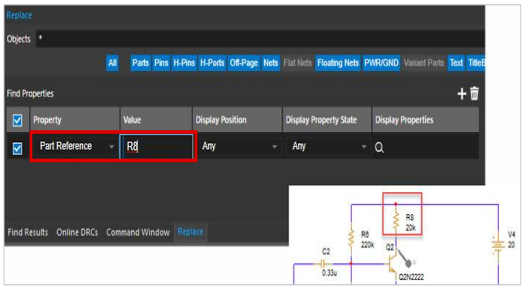
스레드 답변

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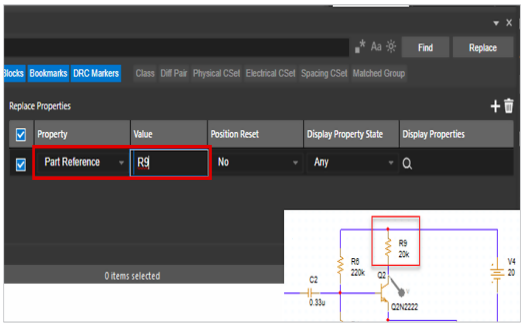
Advanced Find and Replace Properties

회로도 내 객체의 Properties를 검색한 뒤, 일괄 변경하는 기능

- **실행** : Edit > Replace (Ctrl+H)
- **검색 대상** : Parts, Pins, Nets, Text, Class 등 선택
- **사용 방법** : Property, Value 지정 후 Find 실행 → 변경할 Value 입력 후 Replace



Find Properties : Part Reference = R8 검색



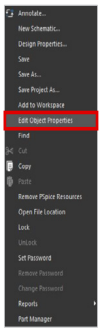
Replace Properties : R9로 변경 후 Replace

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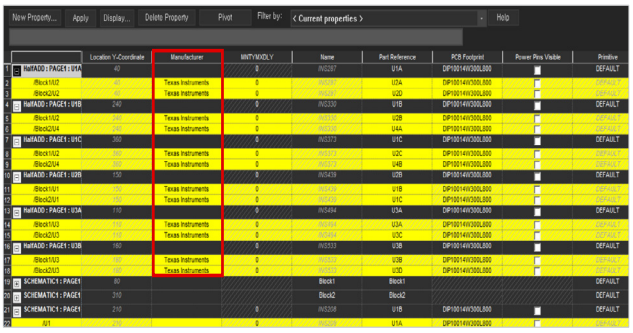
Find and Replace 실습 1. 속성 추가 및 값 입력

74LS 부품에 Manufacturer 속성을 추가하고 값 입력

- **속성 추가** : Project Manager > .dsn 우클릭 > Edit Object Properties > New Property > Manufacturer
- **값 입력** : Edit > Replace > Parts 탭 Value 정렬 > 부품 우클릭 > Edit Properties > Browse Spreadsheet
- **Excel 값 붙여넣기** : Shift + Insert



.dsn 우클릭



Property Editor : Manufacturer 추가 및 값 입력 결과

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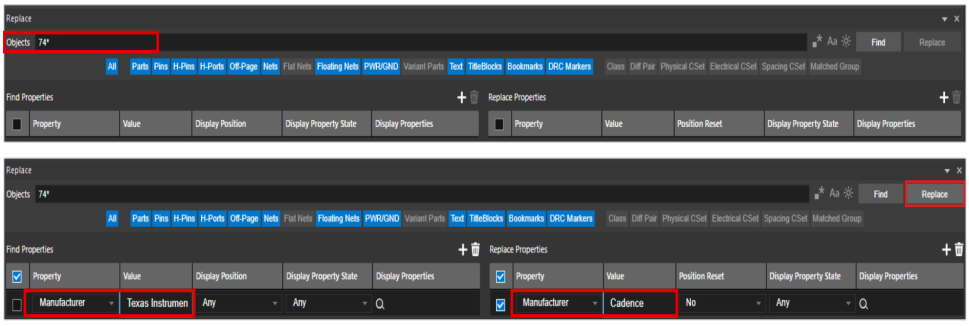
Find and Replace 실습 2. 검색 및 일괄 변경

Edit > Replace (Ctrl+H)에서 부품 검색 후 Manufacturer 값 일괄 변경

- **Objects**: 부품명 검색 (와일드카드 사용 가능, 예: 74*)
- **Find Properties**: + 클릭 > Property = Manufacturer / Value = Texas Instruments (Value는 와일드카드 불가)
- **Replace Properties**: + 클릭 > 변경할 Value 입력 (Cadence) > 상단 Replace 클릭



Edit > Replace



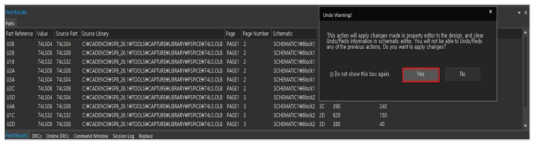
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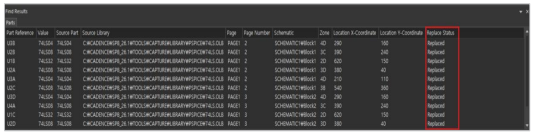
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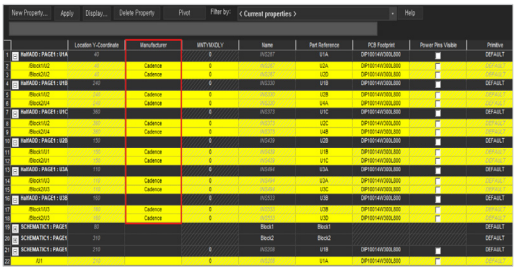
Find and Replace 실습 3. 적용 및 결과 확인

Undo Warning 확인 후 Replace Status, Property Editor에서 결과 확인

- **Replace 실행**: Undo Warning 창에서 Yes
- **결과 확인**: Find Results의 Replace Status = Replaced, Property Editor에서 Manufacturer 변경 확인
- **주의**: Replace 적용 시 Undo/Redo 기록 삭제 → 실행 전 저장 필요







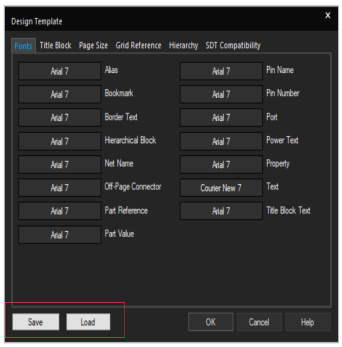
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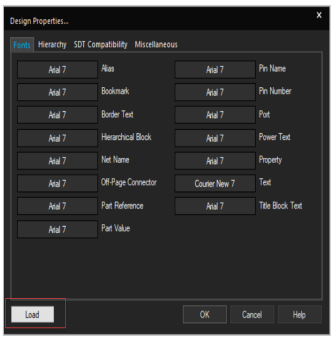
Save and Load Design Template

디자인 템플릿 설정을 .dtp 파일로 저장 후 다른 디자인에서 재사용

- **저장 / 불러오기** : Options > Design Template > Save, Load
- **현재 디자인에 적용** : Design Properties > Load
- **설정 항목** : Fonts, Title Block, Page Size, Grid Reference, Hierarchy, SDT Compatibility
- **버전 호환** : 25.1에서 만든 .dtp → 26.1 적용 가능 / 26.1에서 만든 .dtp → 25.1 적용 가능 (자체 테스트)



Design Template



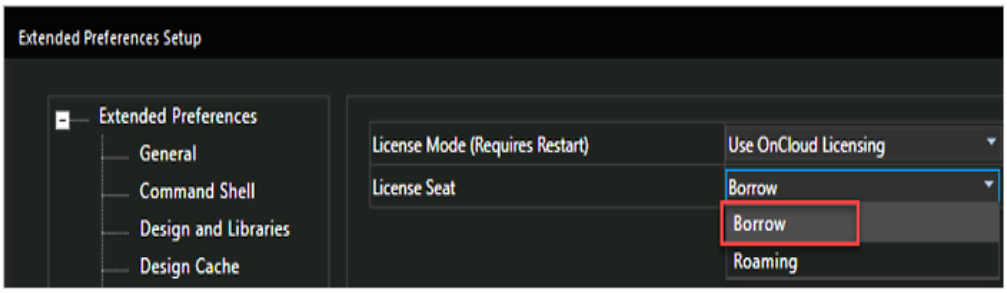
Design Properties

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OnCloud License, 여러 기기에서 사용

OnCloud 라이선스 하나로 최대 5대 설치, 동시 사용은 1대

- **설치** : OnCloud 라이선스 하나로 최대 5대 기기에 설치 가능 (동시 사용은 1대)
- **오프라인 작업** : Extended Preferences Setup > License Seat > Borrow



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OrCAD X Capture Hotfix 010 ~ 050

Hotfix 신규 기능

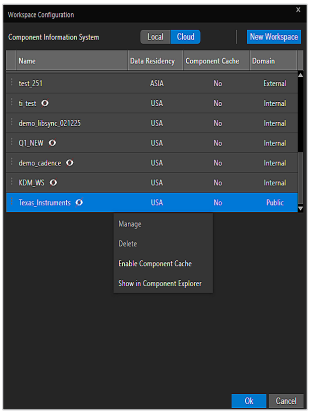
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Access to TI Model Libraries

HF040부터 Component Explorer에서 TI 모델 라이브러리 사용 가능

- **실행** : View > Workspace > Configuration > Texas_Instruments 우클릭 > Show in Component Explorer
- **사용 조건** : OrCAD X Cloud 구독, Windows 1709 이상
- **설치** : 별도 설치 없음 (Cadence Cloud Server에서 자동 다운로드)

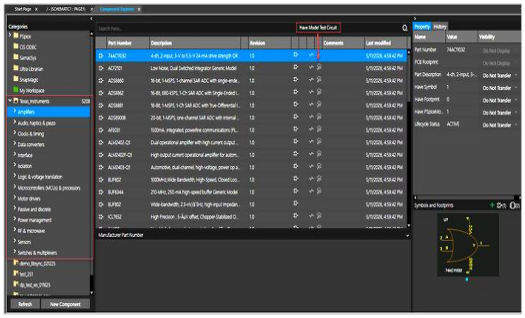


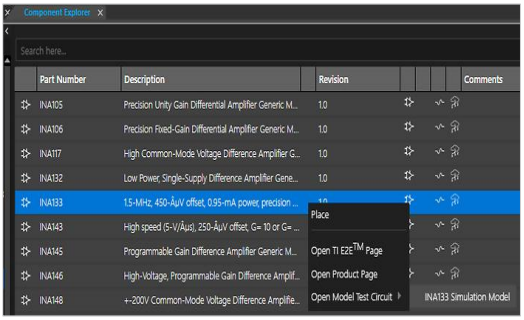
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TI PSpice 모델과 우클릭 메뉴

카테고리별 TI PSpice 모델 확인, 배치 및 테스트 회로 열기

- Component Explorer에서 TI PSpice 모델을 카테고리별로 확인
- **모델 우클릭 메뉴**: Place (회로도에 배치), Open TI E2E Page (TI 지원 페이지), Open Model Test Circuit (테스트 회로 열기)



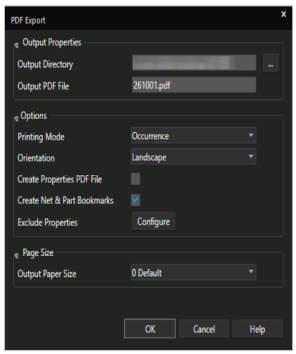


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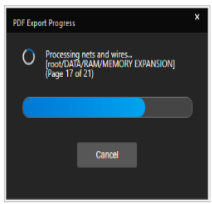
PDF Export Simplified

HF050부터 외부 드라이버 없이 PDF Export 가능

- 외부 드라이버, 수동 설정 없이 PDF Export 가능
- 성능 최적화로 PDF 생성 속도 개선
- Export 시 진행률 창에서 페이지별 처리 상황과 전체 진행률 표시



PDF Export



PDF Export Progress

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정리

Release 26.1 주요 기능 요약

- **26.1** : 25.1 Base ~ HF050에서 추가된 기능을 모두 포함
- **25.1 Base**: Design Review, Advanced Find and Replace, Design Template (.dtp), OnCloud 라이선스 5대 설치 / Borrow
  - **HF040** : Component Explorer에서 TI PSpice 모델 라이브러리 사용
  - **HF050** : PDF Export간소화

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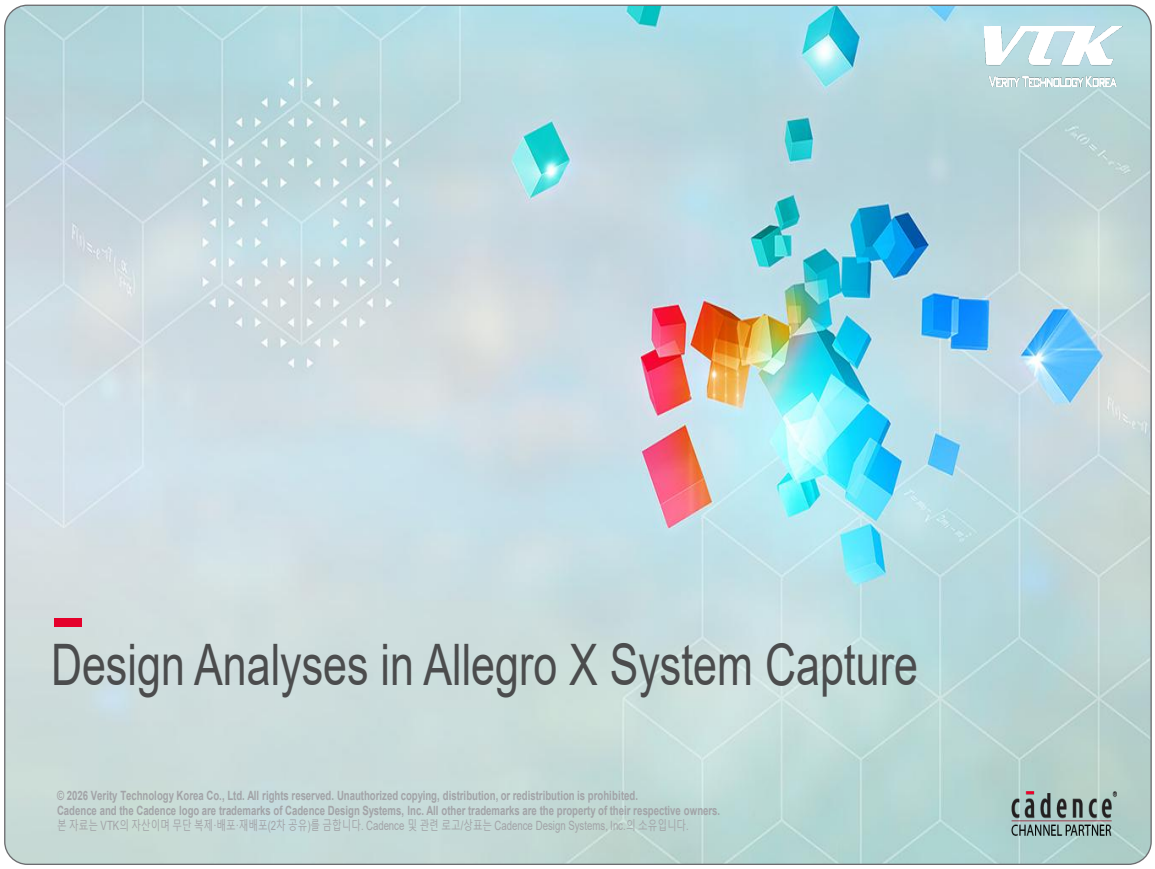
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Design Analyses in Allegro X System Capture & What's New

전 현 우
(Verity Technology Korea)



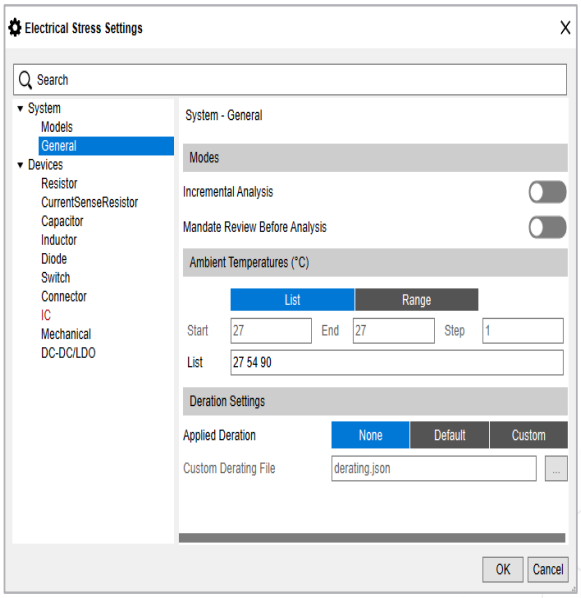
Design Analyses in Allegro X System Capture

- Overview
  - 부품 특성, Design Rule 및 설계 의도를 기반으로 Schematic Design 단계에서 EOS, MTBF, Power Topology, Thermal Analysis 등의 Early Design Analysis를 수행하고, Electrical Stress, Reliability Requirement, Power Delivery, Voltage Margin, Hot Spot, Temperature Margin 등 주요 설계 이슈를 조기에 검증(Shift-Left)
  - 이를 통해 PCB Layout 및 Prototype 이후 발생하는 ECR/ECO 및 PCB Re-spin을 최소화하고, 반복 설계·검증에 소요되는 개발 비용과 Time-to-Market을 단축
  - 향후 AuraStack AI Super Agent를 통해 Allegro X Platform의 설계·구현·Multiphysics Analysis Workflow를 AI Agent 기반으로 연결하고, Electrical / Thermal / Mechanical 분석 결과를 설계에 지속적으로 반영하는 Closed-loop Design Optimization으로 발전

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Design Analyses in Allegro X System Capture

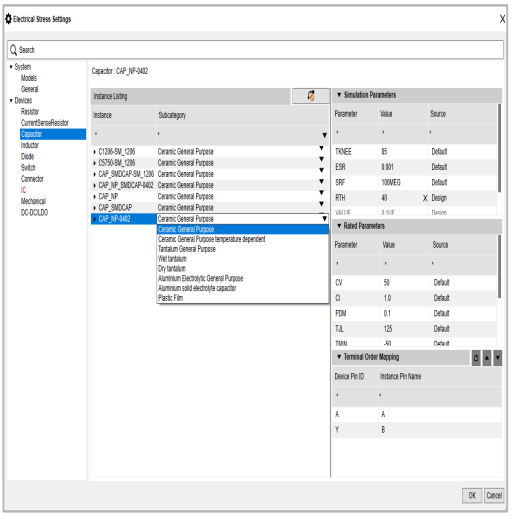
- Analyze Electrical Overstress(EOS)
  - Overview
    - 회로 부품에 인가되는 전압 및 전류 등의 전기적 스트레스를 분석하고, 부품별 허용 스트레스 기준과 비교하여 과부하 위험을 평가
    - Ambient Temperature, Derating, Maximum Value, Stress Level 설정
    - Components에 대한 Model Parameters 세팅
    - 소자 별로 기준 초과 여부를 Results에서 확인
    - Export Results to .csv, .pdf

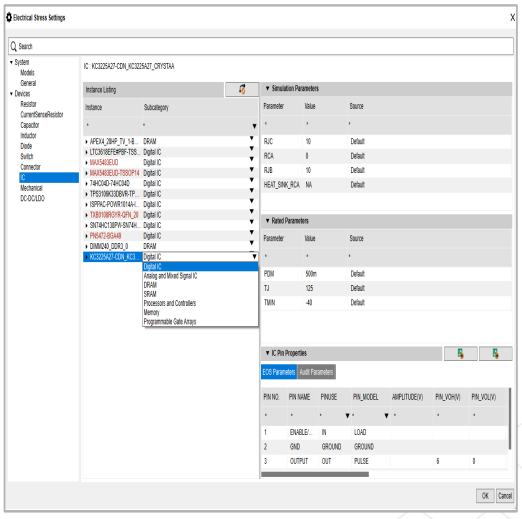


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Design Analyses in Allegro X System Capture

- Analyze Electrical Overstress(EOS)
  - Device Model Parameter Settings(Part Type, Simulation, Derating)
    - Ambient Temperature, Thermal Resistance, Breakdown Temperature, Stress Level, etc

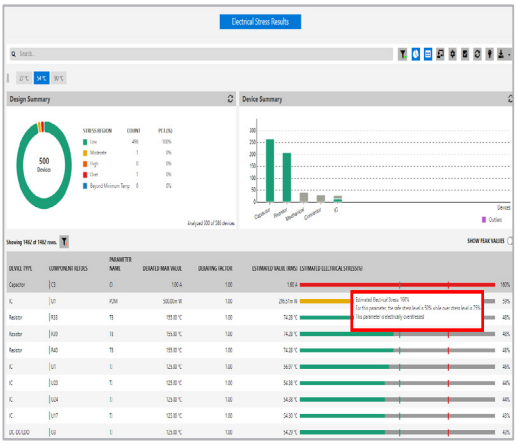




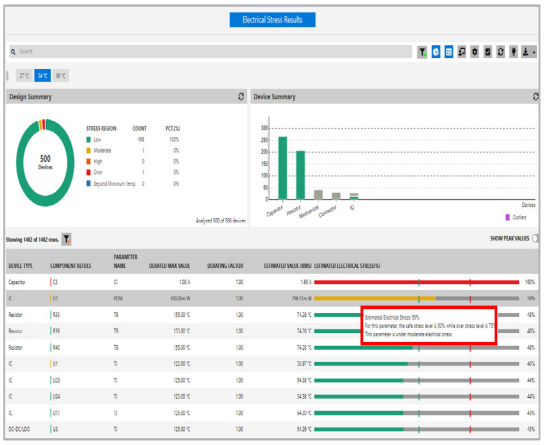
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Design Analyses in Allegro X System Capture

- Analyze Electrical Overstress(EOS)
  - EOS Results



Overstress in 54°C



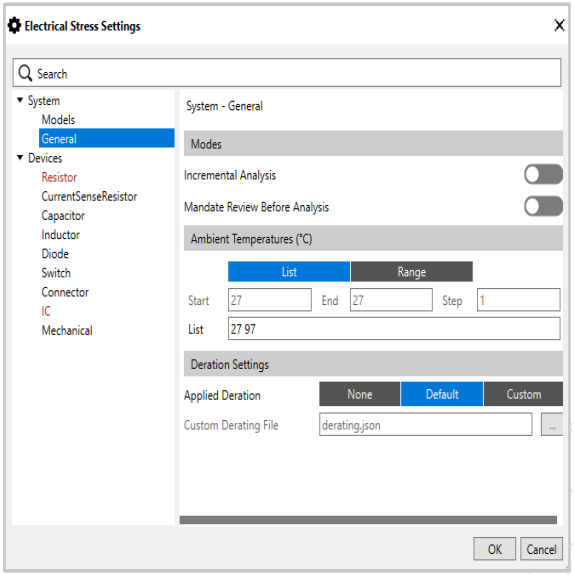
Moderate Stress in 54°C

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Design Analyses in Allegro X System Capture

- Estimate Design MTBF
  - Overview
    - 부품의 신뢰성 모델과 운용 조건 등을 바탕으로 설계된 전자 시스템의 평균 고장 간격을 추정
    - 회로 설계 단계에서 MTBF 분석을 수행하여 부품별 고장률을 기반으로 시스템의 예상 신뢰성을 사전에 평가하고, 신뢰성이 낮은 부품을 조기에 식별
    - 부품 선정 및 회로 설계를 최적화하고, 시제품 제작 이후의 설계 변경 비용과 양산 후 고장 위험을 줄여 제품의 신뢰성을 향상

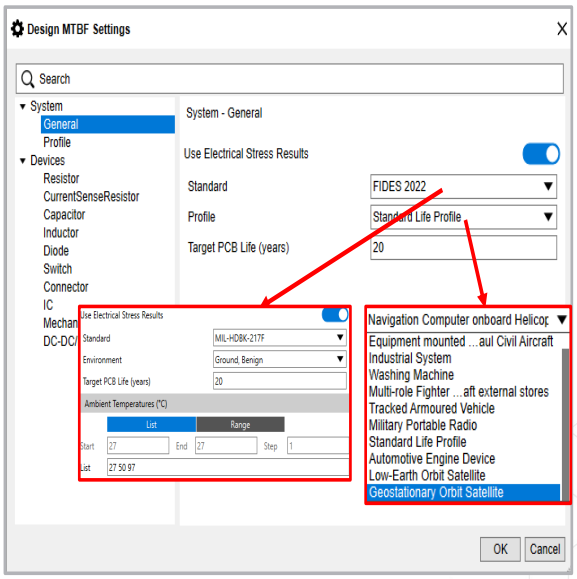


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Design Analyses in Allegro X System Capture

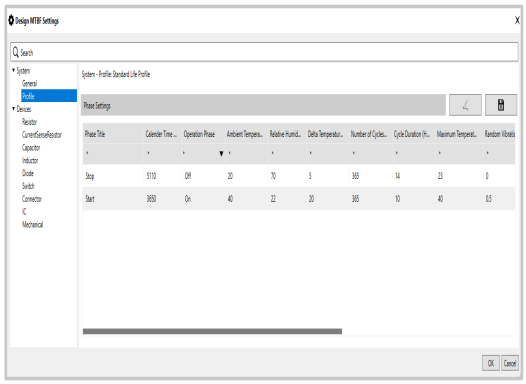
- Estimate Design MTBF
  - Design MTBF Settings
    - 시스템 동작 온도, Environment, Target Life 설정 후 Analysis (MIL-HDBK-217F)
    - EOS Results를 MTBF Estimate에 반영
    - 사용자가 MTBF 예측 모델을 선택
      - MIL-HDBK-217F
      - FIDES 2009
      - FIDES 2022
    - 검증 모델 내 Profile을 지정 후 Analyze
    - 결과값은 .csv, .pdf 형식으로 출력 및 저장

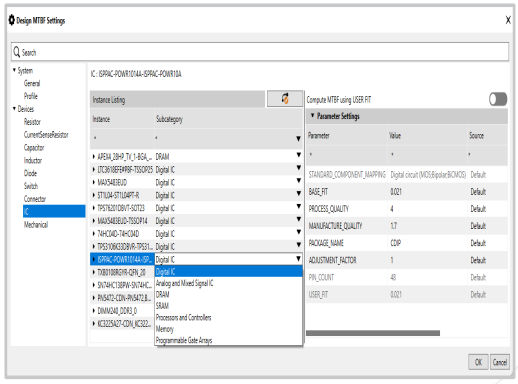


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Design Analyses in Allegro X System Capture

- Estimate Design MTBF
  - Profile and Device Model Parameter Settings
    - Humidity, Temperature, Cycles, Pollution(FIDES)
    - Failure In Time





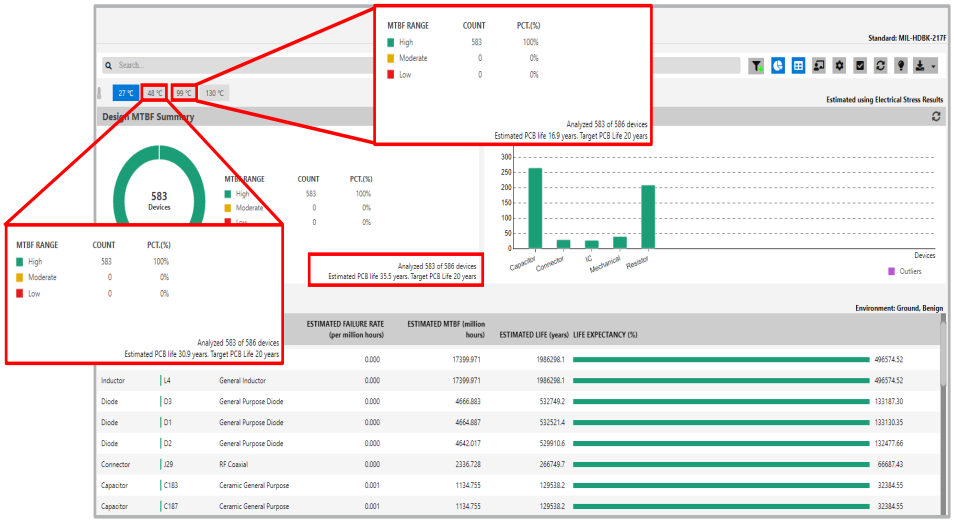
Profile Setting in FIDES

Device Parameters Setting

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Design Analyses in Allegro X System Capture

- Estimate Design MTBF
  - Results MTBF

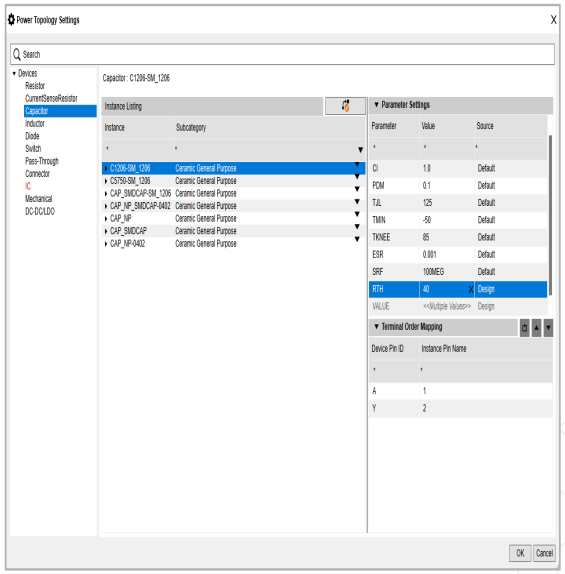


Estimate MTBF By MIL-HDBK-217F

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Design Analyses in Allegro X System Capture

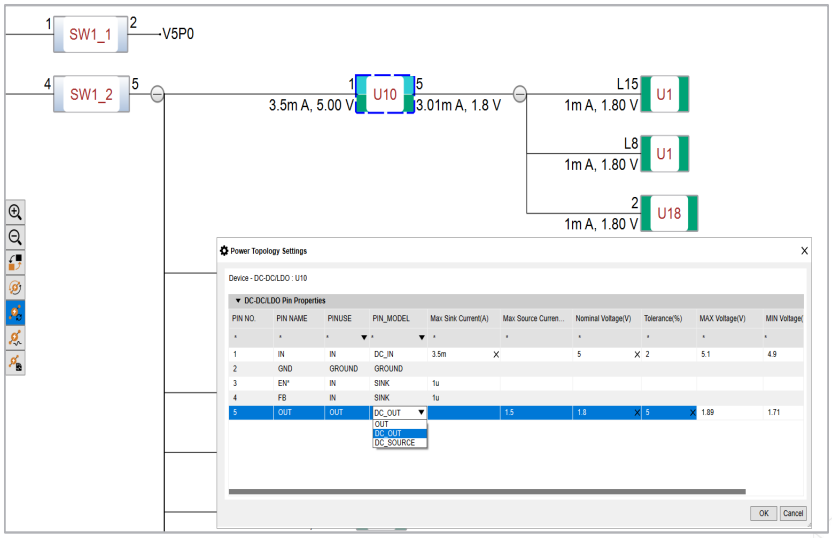
- Power Topology Analysis
  - Overview
    - Pre-Layout 및 Post-Layout 단계에서 DC 전력 분석을 수행하여 전원 공급 경로별 전압·전류 분포, 부품별 전압 강하를 분석하고, 설계 기준에 따른 Pass/Fail 검증 수행
    - 회로도 데이터를 기반으로 전원 공급 네트워크의 토폴로지를 구성하여 전원 공급원부터 소비 부품까지의 전력 전달 경로와 전원 분배 구조를 시각화하고 분석
    - IR Drop, Current Density 등 주요 설계 기준의 초과 여부를 조기에 식별하여 전원 공급 경로의 문제점을 파악하고, 설계 검토 효율성 및 신뢰성 향상
    - Power Topology Analysis 진행 전, Model Parameter default setting



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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Pre-Layout Analysis
    - Setting Power Rail

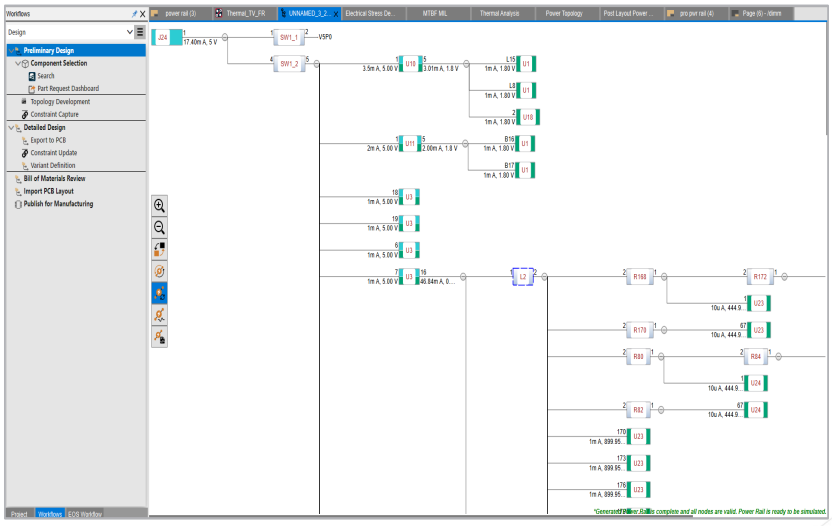


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Pre-Layout Analysis
    - Build Power Tree

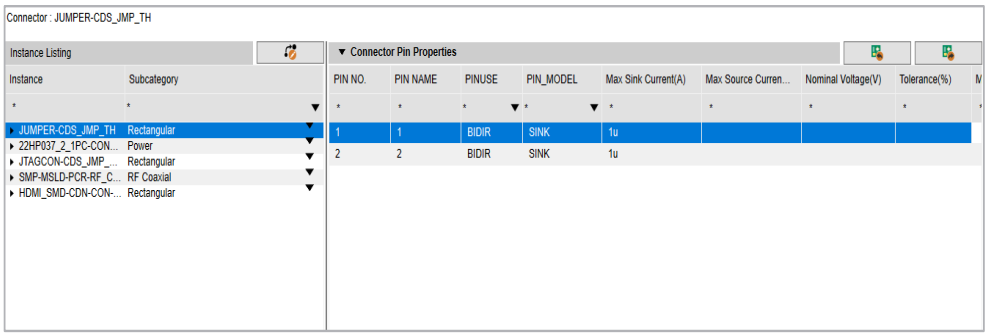


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Pre-Layout Analysis
    - Toggle SINK(View Only SINK PIN MODEL)

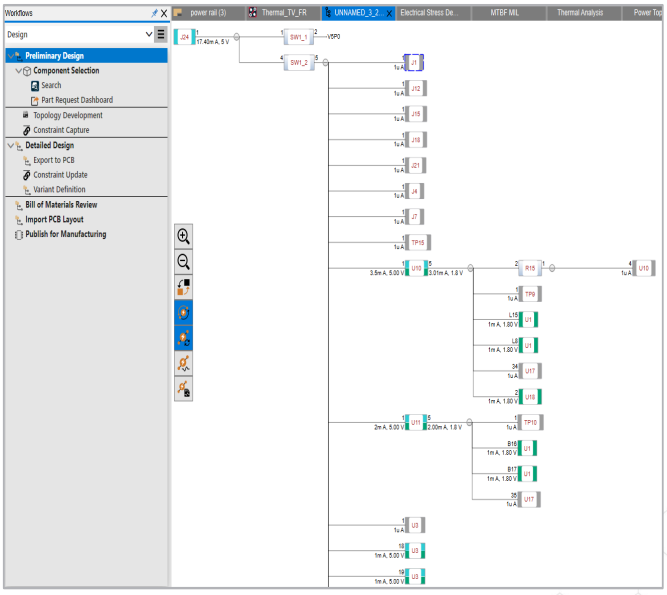


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Pre-Layout Analysis
    - Toggle SINK(View Only SINK PIN MODEL)
    - Power Pin is displayed in a green box
    - Sink Pin is displayed in a grey box

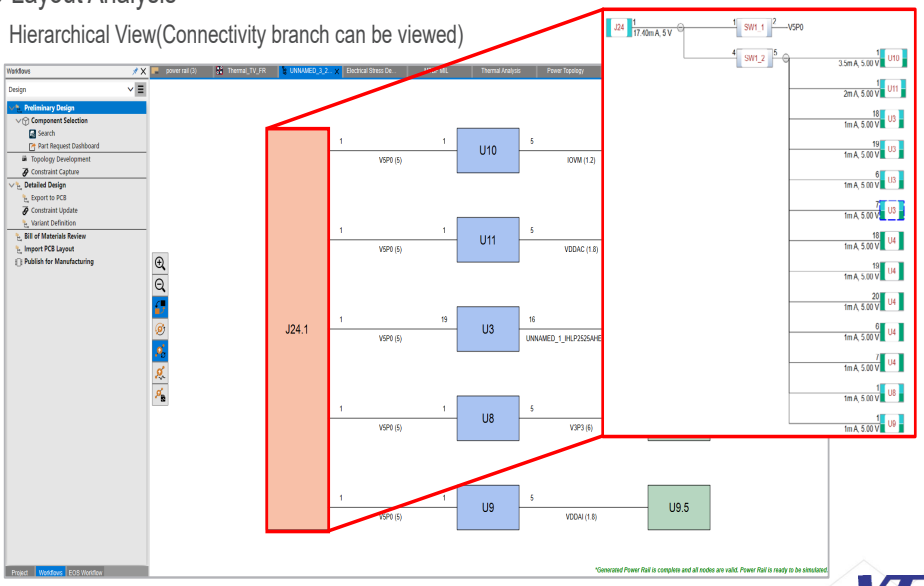


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Pre-Layout Analysis
    - Hierarchical View(Connectivity branch can be viewed)

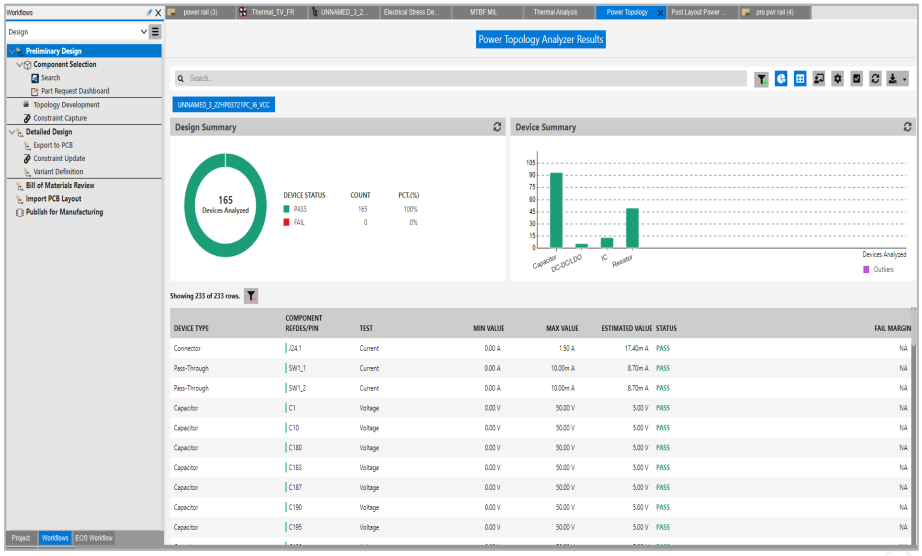


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Pre-Layout Analysis Results

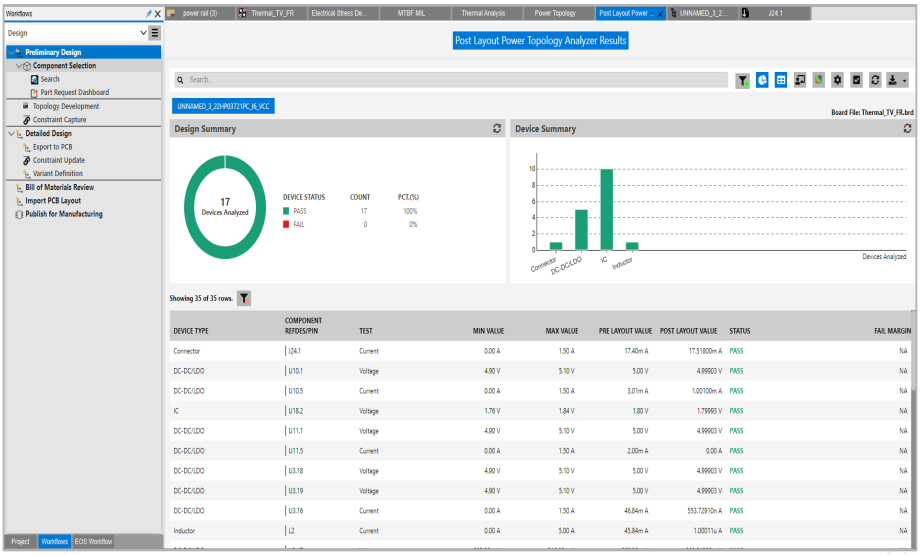


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Post-Layout Analysis Results

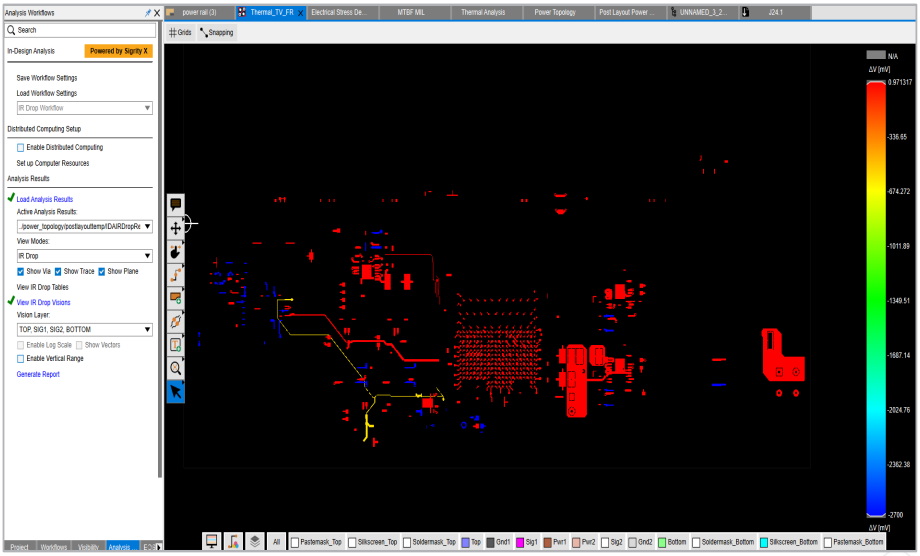


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Post-Layout Analysis Results

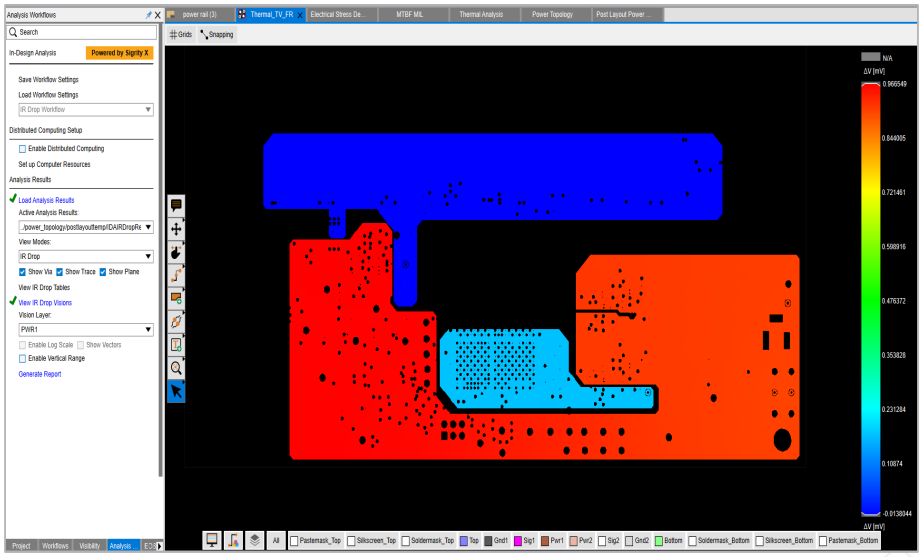


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Post-Layout Analysis Results(IR Drop)

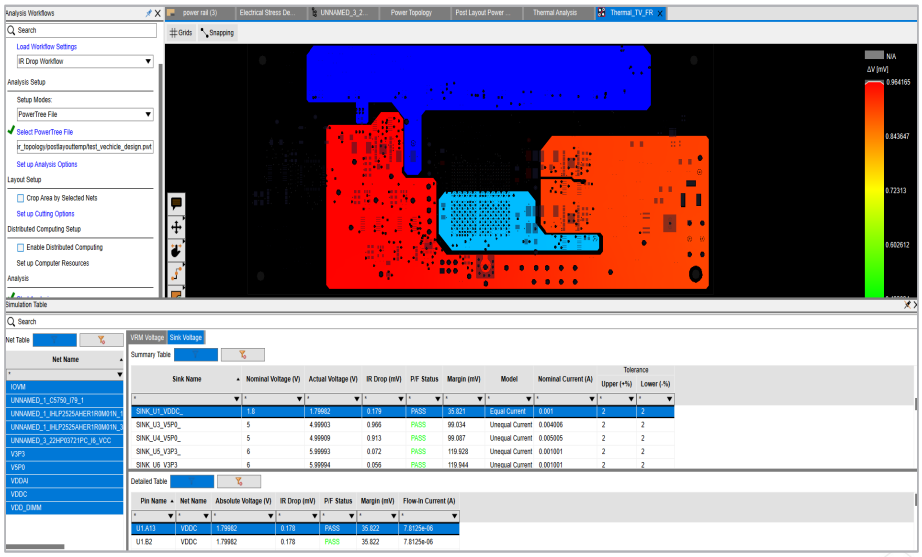


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Post-Layout Analysis Results(IR Drop)

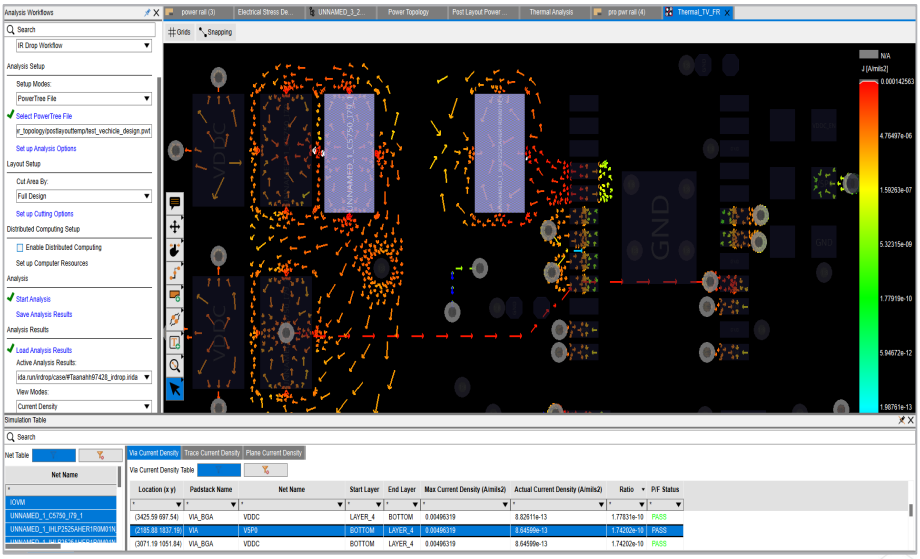


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Post-Layout Analysis Results(Current Flow)

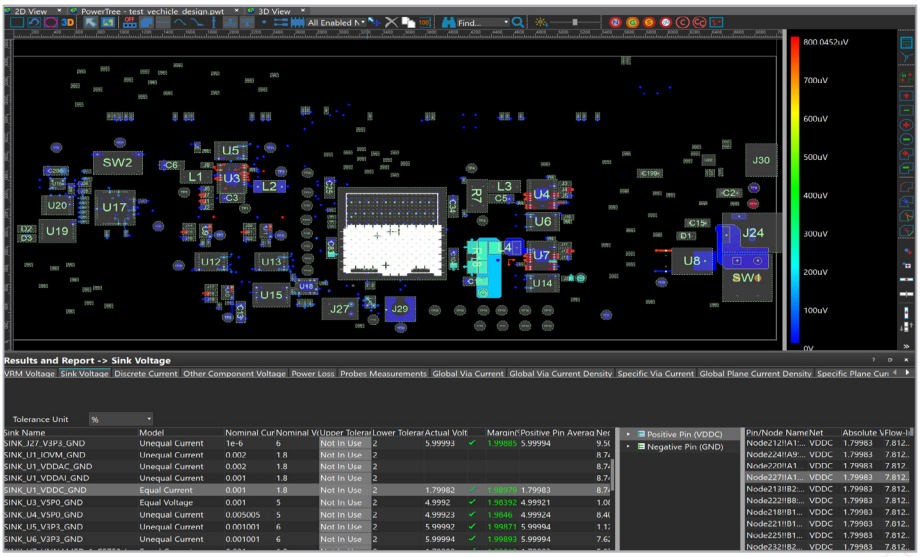


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Post-Layout Analysis Results(In Layout Workbench)

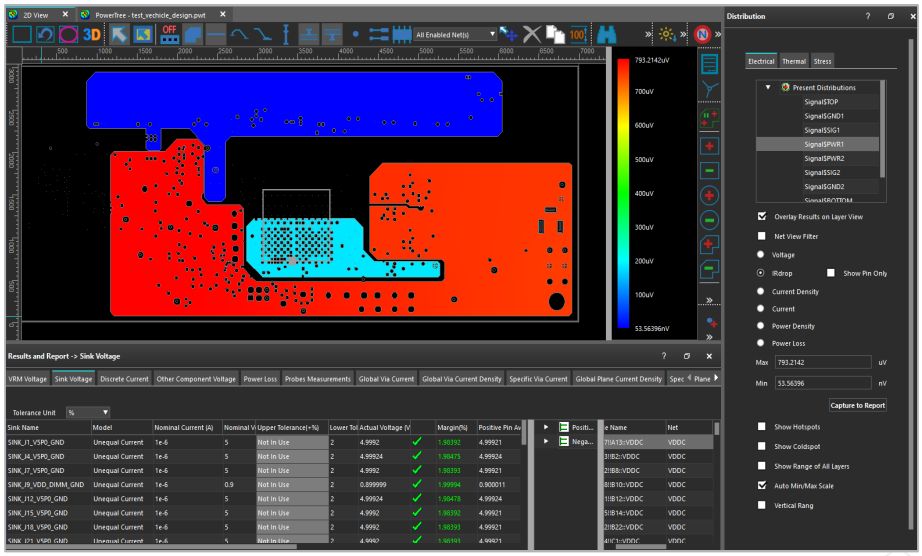


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Design Analyses in Allegro X System Capture

- Power Topology Analysis
  - Post-Layout Analysis Results(In Layout Workbench)

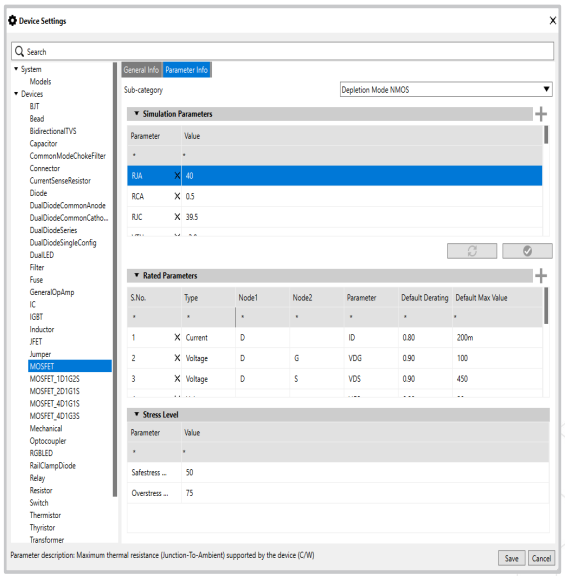


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Design Analyses in Allegro X System Capture

- Thermal Analysis
  - Overview
    - 회로 및 PCB의 발열과 온도 분포를 분석하여 부품의 열적 설계 적합성을 평가
    - 과열 및 Hotspot을 조기에 식별하고, 방열 설계를 최적화하여 부품의 열적 안정성과 제품 신뢰성을 향상
    - Ambient Temperature, Derating, Maximum Value, Stress Level 설정 후, Analysis 진행
    - 각 Device 별로 설정한 RefDes Prefix 기반으로 회로상에서 부품 식별 후, Default 설정한 Model Parameter 적용
    - Device 별 Sub-Category로 적용할 Model 설정

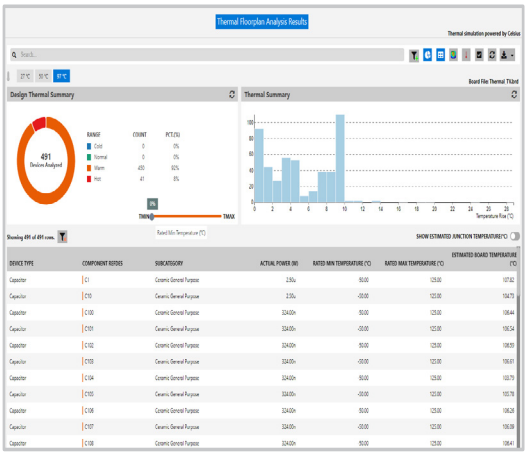


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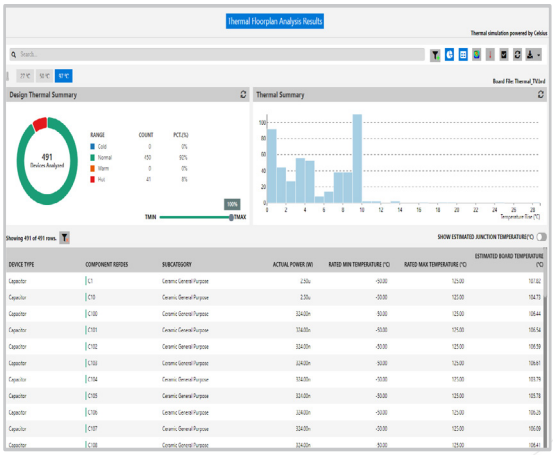
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Design Analyses in Allegro X System Capture

- Thermal Analysis
  - Results about Thermal Analysis



Rated Min Temperature in 97°C



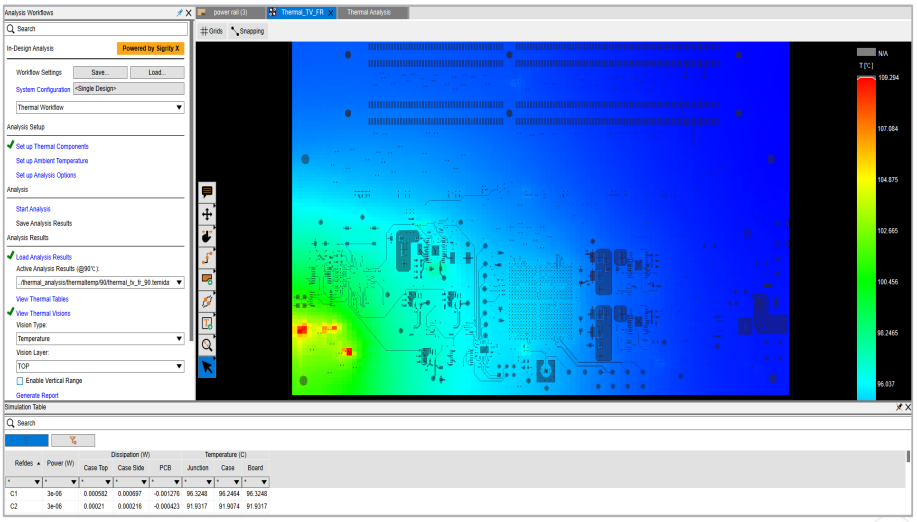
Rated Max Temperature in 97°C

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Design Analyses in Allegro X System Capture

- Thermal Analysis
  - Thermal Analysis Workflow
    - View Thermal Map and Simulation Table



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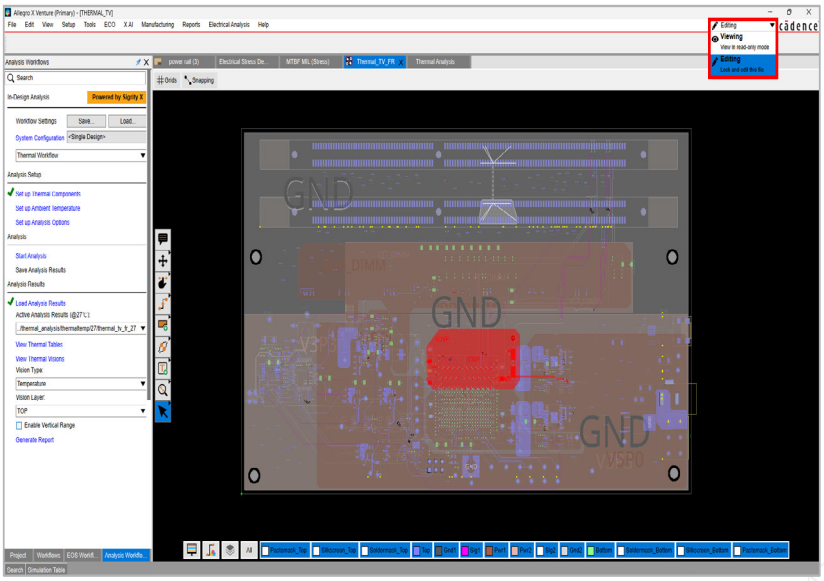
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What's New

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What's New

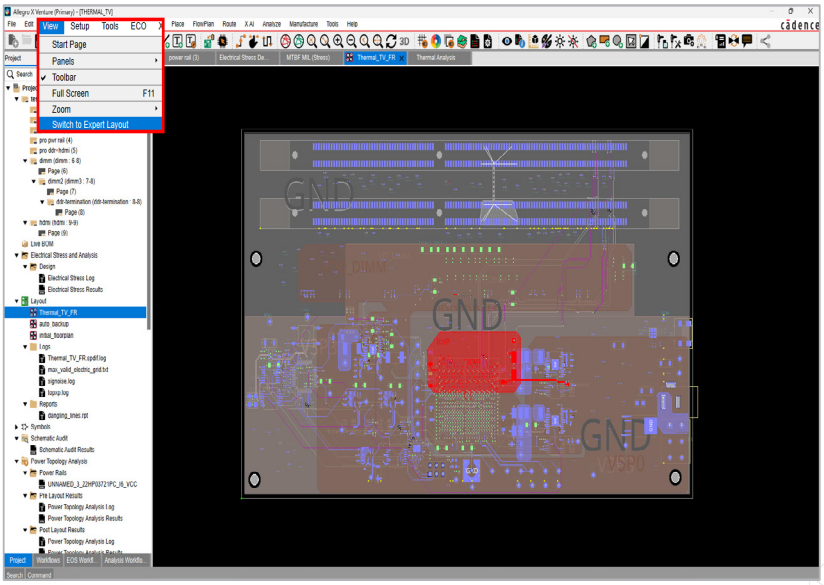
- PCB Artwork in System Capture
  - OrCAD X Presto UI



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What's New

- PCB Artwork in System Capture
  - Allegro X PCB Editor UI

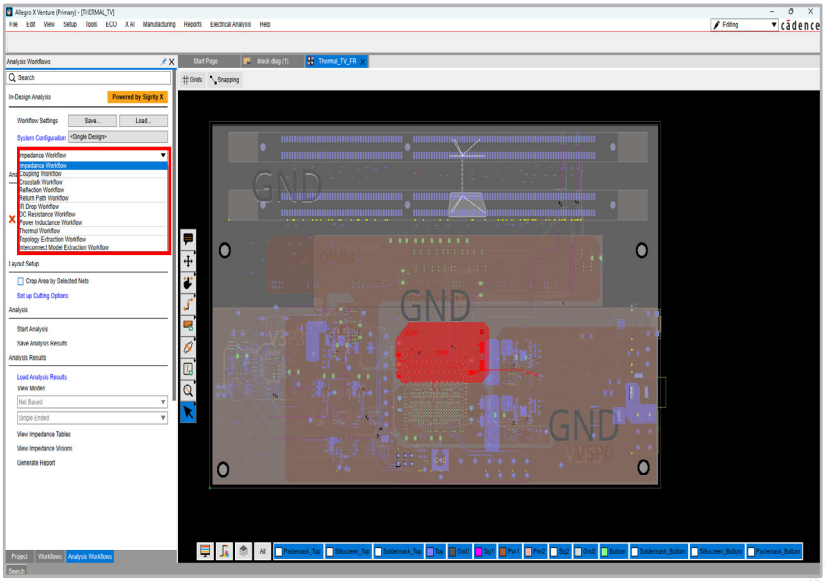


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What's New

- PCB In-Design Analysis in System Capture
  - IDA Workflow(Sigrity X Aurora PCB Analysis)

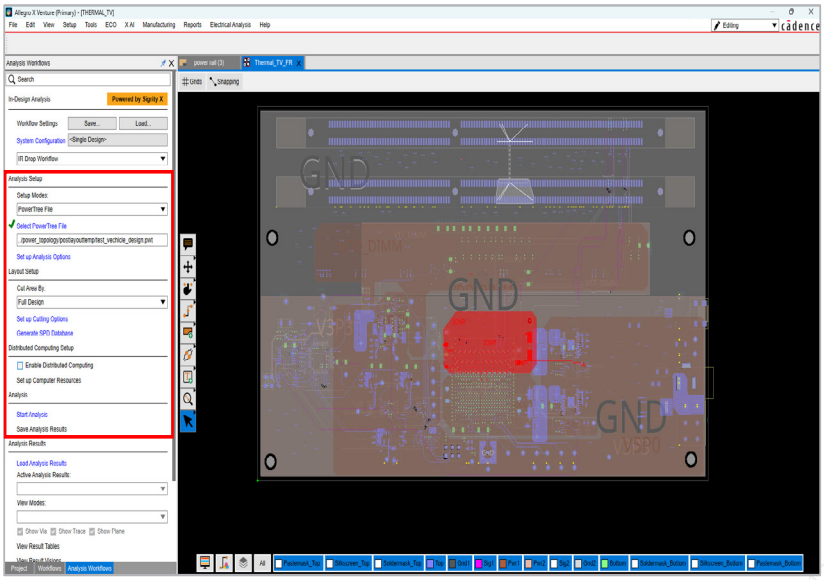


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What's New

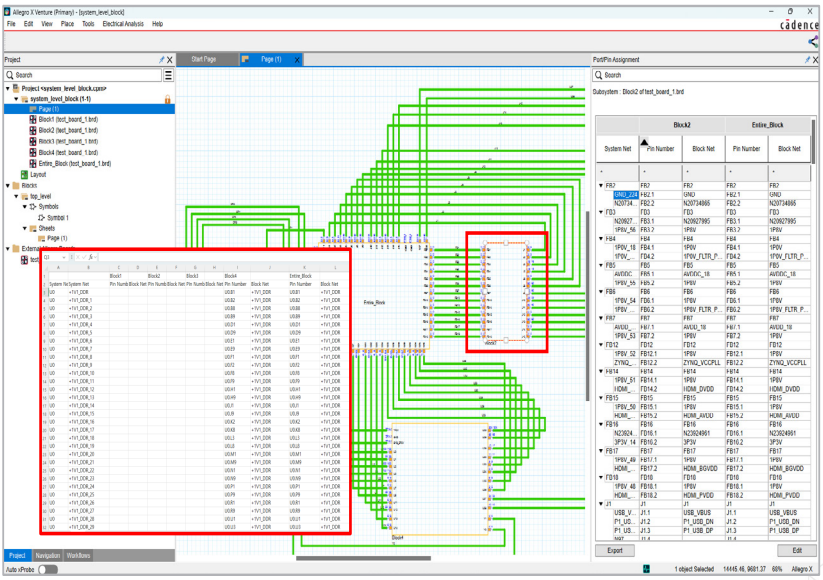
- PCB In-Design Analysis in System Capture
  - IDA Workflow(Sigrity X Aurora PCB Analysis)



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What's New

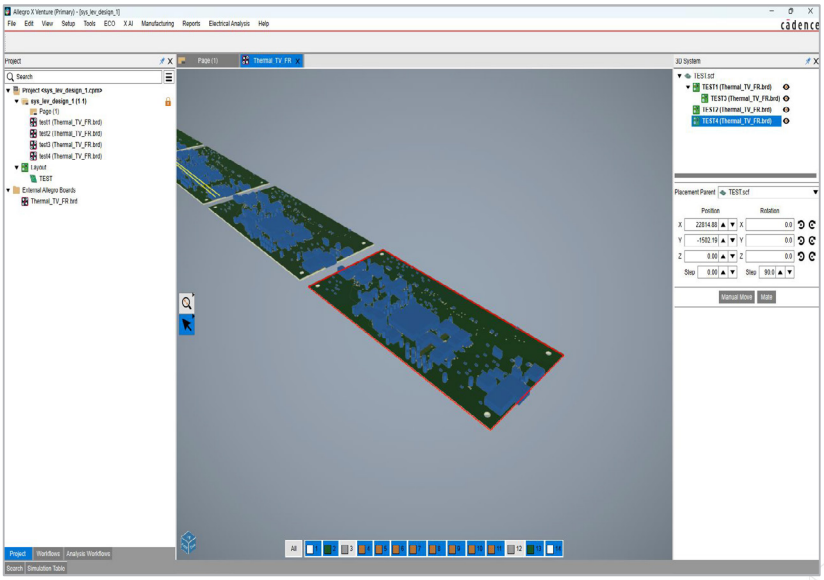
- System-Level Design in System Capture
  - Import External Allegro Board(.brd, .mcm, .mdd)



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What's New

- System-Level Design in System Capture
  - Export to 3D System View(Only .brd)



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PSpice What's New & Key Feature Highlights

공 연 희
(Verity Technology Korea)



Agenda

PSpice What's New & Key Feature Highlights

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- Persona-Based Configuration
- Convergence Error Debugging

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- Nonlinear Passive Modeling
- .MEASURE Command

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Simulation Setup & Debugging

01 시뮬레이션 설정 및 디버깅

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Accelerate Simulation Setup with Persona-Based Configuration

Persona란? PSpice 23.1

허용 오차 · 반복 횟수 등 시뮬레이션 옵션을 **회로 용도에 맞게 미리 묶어둔 설정**

1 PSpice.ini · Persona 정의

```
[PSPICE PERSONAS]
GENERAL_RELAXED=RELTOL=0.01,ABSTOL=10n,VNTOL=0.001,ITL1=1000,ITL2=500,ITL4=50
SWITCHING_CIRCUITS=ITL1=1000,ITL2=1000,ITL4=40,RELTOL=0.005,ABSTOL=1.0n,VNTOL=10u
DC_ANALYSIS=ITL1=1000,ITL2=100,PTRANABSTOL=20u,PTRANVNTOL=0.1m,STEPGMIN,PREORDER
SEMICONDUCTOR_JUNCTION=DIODES=0.1m,DIODEJCJO=2p,BJTCJ=10p
AUTOCONVERGENCE=AUTOCONVERGE,ITL1=1000,ITL2=1000,ITL4=100,RELTOL=0.05,ABSTOL=1.0E-6,
```

파일 위치

```
%home%\cdssetup\OrCAD_PSpice\26.1.0
```

Persona 선택 시 적용

2 Simulation Profile · 설정 적용

- Analog Simulation
  - General
  - Auto Converge
  - MOSFET Option
- Analog Advanced
  - General
  - Bias Point
  - Transient
- Gate Level Simulation
  - General
  - Advanced
- Output File
  - General

Name	Value	Default Value
SELECTED_PERSONA	Default	Default
SPEED_LEVEL	3	3
RELTOL	0.001	0.001
VNTOL	1.0u	1.0u
ABSTOL	1.0p	1.0p
CHGTOL	0.01p	0.01p
GMIN	1.0E-12	1.0E-12
ITL1	150	150
ITL2	20	20
ITL4	10	10
TNOM	27.0	27.0
THREADS	0	0

기본 제공 Persona

GENERAL_RELAXED | SWITCHING_CIRCUITS | DC_ANALYSIS | SEMICONDUCTOR_JUNCTION | AUTOCONVERGENCE

ini에 정의된 옵션 값을 프로파일에 일괄 적용

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Accelerate Simulation Setup with Persona-Based Configuration

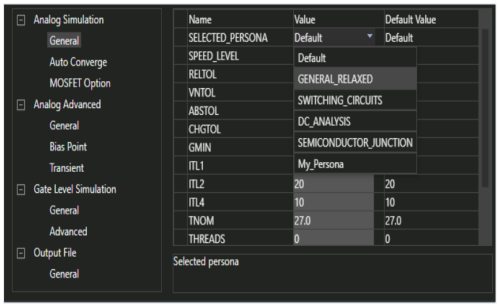
페르소나 사용의 간편화 PSpice 26.1

명령어 · 텍스트 입력

```
@PSpice:
.PERSONA SWITCHING_CIRCUITS
```

- Persona 이름을 직접 입력
- 명령어 선언 필요

Simulation Profile에서 간편 선택



- 드롭다운 선택만으로 **정의된 시뮬레이션 옵션 자동 적용**

명령어 입력 없이 Simulation Profile에서 선택만으로 Persona 적용

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Enhanced Debugging of Convergence Error

Convergence Error 디버깅 기능 향상 PSpice 23.1

Convergence Error란?

회로 시뮬레이션 중 **시뮬레이터가 해를 찾지 못하는 경우**에 발생하는 오류

주요 원인

1. 비정상적으로 높거나 낮은 값
2. 부동소수점 오류 Floating-point error
3. 복잡한 회로 내 비현실적이거나 과도한 계산식

.OPTIONS EXPR_DEBUG

수렴 오류를 유발하는 **수식**을 경고 메시지에 포함하여 출력

```
@PSpice:
.OPTIONS EXPR_DEBUG
```

옵션 선언 → 시뮬레이션 실행 → **원인 수식 경고 표시**

수렴 오류의 원인이 되는 수식을 경고 메시지로 바로 확인

오류의 원인을 더 쉽게 식별

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Libraries & Sources

02 라이브러리 및 소스 확대

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Additional Component Libraries Available in PSpice

PSpice 모델 · 소스 지원 확대 (23.1 → 26.1)

23.1

자동차 과도 소스 도입

지원 표준

ISO 7637-2 · ISO 16750-2

사용 경로

Component Explorer › PSpice › Source › **Automotive Pulses**

라이브러리

`automotivesrc.olb`

25.1

자동차 시험 · GaN 모델 확대

ISO 16750-2 · 12V / 24V

Single Line Interruption, Load Dump Test A / B

CI 210

연속 AC 외란 내성 시험 소스

GaN MOSFET

OrCAD X Capture · Discrete에서 제공

26.1

수동소자 라이브러리 확대

TAIYO YUDEN · Murata

커패시터 · 인덕터 등 수동소자

10,000+ 신규 모델

48,000+ 전체 제공 모델

제공 방식

기본 설치 · PSpice Search 통합
심볼 + SPICE 모델 또는 모델 단독

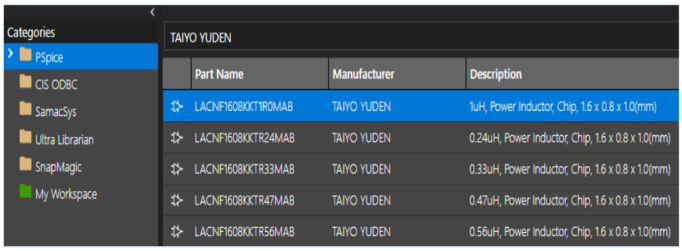
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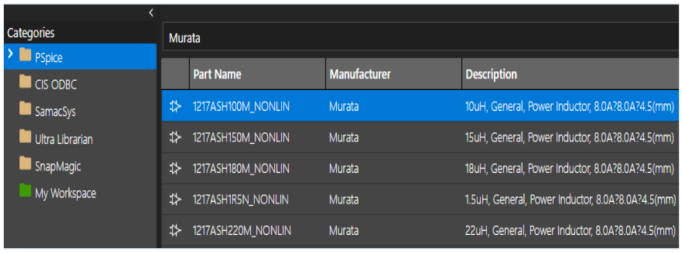
Additional Component Libraries Available in PSpice

Component Explorer에서 확인한 Additional Component

TAIYO YUDEN



Murata



확인 방법

1. Categories에서 **PSpice** 선택
2. **Manufacturer** 열에서 제조사 확인
3. **Description**에서 소자 사양 확인

예시 · Power Inductor

TAIYO YUDEN	LACNF1608 시리즈
Murata	1217AS 시리즈

10,000+ 신규 수동소자 모델
기본 설치로 바로 사용

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Support for Automotive Transient Sources

자동차 전장용 Transient Source 버전별 지원 확대

PSpice 23.1

표준 Transient Source 도입

ISO 7637-2 · ISO 16750-2

배치 방법

Component Explorer › PSpice › Source

Automotive Pulses 신규 카테고리

라이브러리에서 직접 배치

```
<install_dir>\tools\capture\library\pspice\automotivesrc.olb
```

PSpice 25.1

시험 항목 확대

12V / 24V 차량 전원 시스템

ISO 16750-2 추가 시험 항목

- 4.9.1 Single Line Interruption 전원 순간 단선
- 4.6.4 Load Dump Test A 중앙 억제 회로 미적용
- 4.6.4 Load Dump Test B 중앙 억제 회로 적용

CI 210

연속 교란 AC 내성 시험용 소스 추가 Continuous Disturbance

23.1 표준 소스 도입 → 25.1 시험 항목 세분화 및 CI 210 추가

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Model Management

03 모델 활용 및 보안

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Model Sweep & Conditional Model Selection

모델 스윕 및 조건부 모델 선택

Model Sweep PSpice 25.1

기능
모델 목록에 따른 순차 해석

적용 방식
동일 회로의 기준 모델을 대체 모델로 교체하여 반복 해석

활용
모델별 회로 특성 비교 및 설계 대안 검토

MODEL LIST

```
MODEL_A
MODEL_B
MODEL_C
```

IFTEXT PSpice 26.1

기능
조건식에 따른 모델 선택

적용 방식
파라미터 조건을 평가하여 적용할 모델 이름 결정

활용
설계 조건에 따른 모델 구성 관리

EXPRESSION

```
{IFTEXT(VC==28,
   "Q2N2222A", "Q2N5551")}
```

모델 목록 순차 비교 Model Sweep · 조건식 기반 자동 선택 IFTEXT

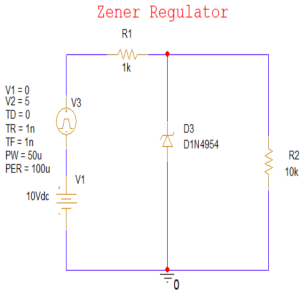
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Model Sweep PSpice 25.1

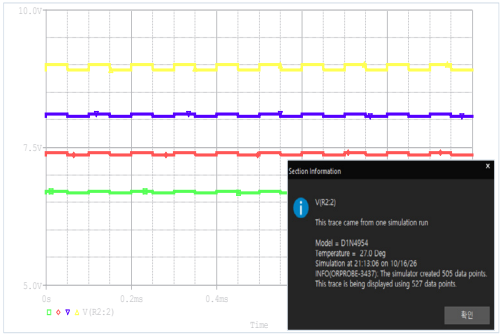
회로에서 모델별 시뮬레이션 결과 비교

시뮬레이션 회로




```
@PSpice:
.modelstep d1n4954 d1n4955 d1n4956 d1n4957
```

모델별 출력 전압 비교



Probe 창에서 모델별 결과를 한 번에 확인

한 번의 실행으로 여러 모델의 결과를 비교

회로는 유지하고 기준 모델을 순차적으로 교체하여 해석

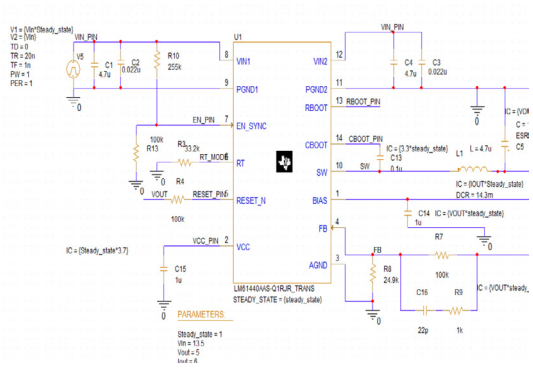
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Conditional Model Selection

조건부 모델 선택 · IFTEXT PSpice 26.1

예제 회로도



LM614x0 Buck Converter 예제 회로

모델의 Recommended Operating Condition 비교

LM61440-Q1 Load current 0 ~ 4 A

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted) [1]

		MIN	NOM	MAX	UNIT
Input voltage	Input voltage range after start-up	3		36	V
Output voltage	Output voltage range for adjustable version [2]	1		0.95 * V_{IN}	V
Frequency	Frequency adjustment range	200		2200	kHz
Sync frequency	Synchronization frequency range	200		2200	kHz
Load current	Output DC current range [3]	0		4	A
Temperature	Operating junction temperature T_J range	–40		150	°C

LM61460-Q1 Load current 0 ~ 6 A

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted) [1]

		MIN	NOM	MAX	UNIT
Input voltage	Input voltage range after start-up	3		36	V
Output voltage	Output voltage range for adjustable version [2]	1		0.95 * V_{IN}	V
Frequency	Frequency adjustment range	200		2200	kHz
Sync frequency	Synchronization frequency range	200		2200	kHz
Load current	Output DC current range [3]	0		6	A
Temperature	Operating junction temperature T_J range	–40		150	°C

Load Current 범위에 따라 적용할 모델 Sweep

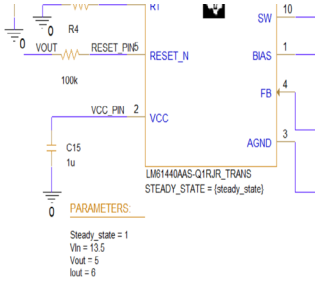
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Conditional Model Selection

부하 조건에 따른 Buck Converter 선택 · IFTEXT

Parameters 변수 설정




```
{IFTEXT(Iout<=4, "LM61440AAS-Q1_TRANS",
        "LM61460AAS-Q1_TRANS")}
```

설계 조건에 따른 모델 선택

	부하 조건	적용 모델
IC	Iout ≤ 4 A	LM61440-Q1
IC	4 A < Iout ≤ 6 A	LM61460-Q1

예제 설정 `Iout = 6` → LM61460-Q1 적용

Parameter 값에 따라 조건에 맞는 모델이 자동 적용

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Conditional Model Selection

Parametric Sweep을 이용한 조건별 비교 · IFTEXT

스윕 설정

Global parameter

`Iout`

Value List

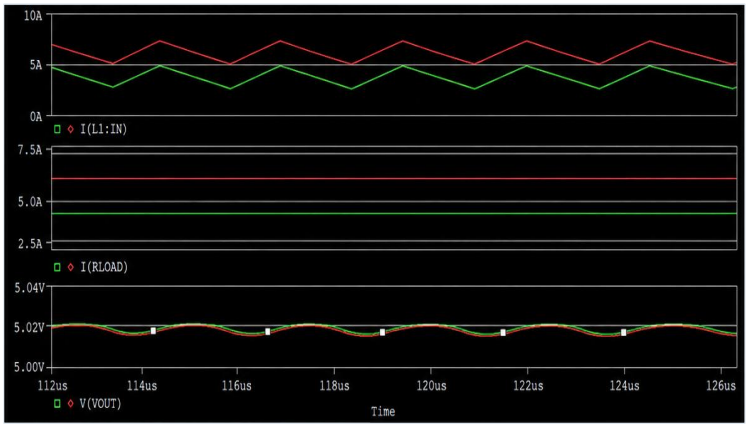
`4  6`

4 A	LM61440-Q1
6 A	LM61460-Q1

각 스윕 조건에서 모델 자동 선택

시뮬레이션 결과

Iout = 4 A / 6 A 순차 해석, 동일 Probe 창에서 확인



부하 조건과 모델을 함께 변경하고 결과를 한 화면에서 비교

인덕터 전류 I(L1:IN) · 부하 전류 I(RLOAD) · 출력 전압 V(VOUT)

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Enhanced Encryption Security for PSpice Model Libraries

모델 암호화 보안 강화

기존 방식

기존 암호화

- DES 및 AES 기반 암호화 지원
- 모델 정보를 보호하며 시뮬레이션 가능
- Model Editor의 Encrypt Library 사용

강화된 암호화 엔진

PSpiceEnc

명령 프롬프트 실행

PSpice 25.1

업데이트된 암호화

- 강화된 암호화 엔진으로 보안 향상
- 기존 암호화 라이브러리 재암호화 지원
- 기존 명령어와 인자 그대로 사용

기존 명령어와 인자 그대로 더 강력한 암호화 적용

기존에 암호화한 라이브러리도 PSpiceEnc로 재암호화 가능

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Enhanced Encryption Security for PSpice Model Libraries

라이브러리 암호화 방법

1 기존 라이브러리 암호화

Model Editor에서 Encrypt Library 실행

Model Editor → Encrypt Library → 암호화 파일 생성

2 강화된 방식으로 재암호화 PSpice 25.1

명령 프롬프트에서 설치 디렉터리로 이동 후 실행

설치 경로로 이동

```
cd %CDSROOT%\tools\bin
```

기존 암호화 라이브러리 재암호화

```
PSpiceEnc  C:\Models\old_enc.lib  C:\Models\enhanced_enc.lib
```

`old_enc.lib` 기존 암호화 파일 `enhanced_enc.lib` 강화된 암호화 결과 파일

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Modeling & Measurement

04 고급 모델링 및 측정

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Support for Advanced Capabilities in PSpice

비선형 수동소자 모델 지원

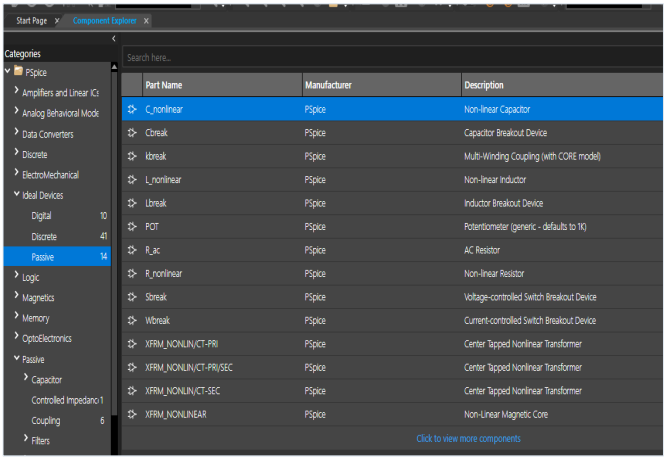
수학식을 이용한 비선형 수동소자 모델링

Directory

Component Explorer › PSpice › Ideal Devices › **Passive**

주요 소자

`C_nonlinear`	Non-linear Capacitor
`L_nonlinear`	Non-linear Inductor
`R_nonlinear`	Non-linear Resistor
`R_ac`	AC Resistor



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수학식을 활용한 비선형 수동소자 모델링

NTC 예제: 온도에 따른 저항 특성을 수식으로 정의하고 시뮬레이션으로 확인

1 특성식 정의

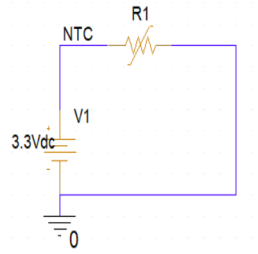
25°C에서 100 kΩ, B = 3977 K인 NTC 모델

$$R(T) = 100k \times \exp[3977 \times (1/(T+273.15) - 1/298.15)]$$

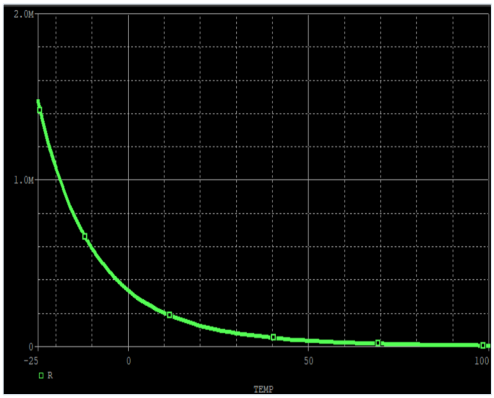
T: 섭씨 온도(°C), 식 내부에서 켈빈으로 변환

2 R_Nonlinear에 수식 적용

```
{100k*EXP(3977*(1/(TEMP+273.15)-1/298.15))}
```



3 온도 스윕 결과



−25°C	25°C
약 1.47 MΩ	100 kΩ

온도 상승에 따라 저항이 감소하는 **NTC 특성 재현**

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.MEASURE (Transient, AC, and DC Analysis)

시뮬레이션 결과를 자동으로 측정하는 .MEASURE 명령어

Transient · AC · DC 해석의 출력 데이터를 **시뮬레이션 실행 중 바로 측정** · 해석 유형은 Simulation Profile에서 자동으로 읽음

```
.MEAS[URE] {DC|AC|TRAN} result + <측정 구문>
```

DC|AC|TRAN 생략 가능 (마지막 해석과 동일)

TRIG ··· TARG

트리거 시점부터 타깃 시점까지의 시간 측정

```
+ TRIG v1 VAL=val <RISE=#>
+ TARG v2 VAL=val <FALL=#>
```

FIND ··· WHEN

조건이 성립하는 시점의 출력값 측정

```
+ FIND out_variable
+ WHEN out_var2 = val
```

AVG · RMS · MIN · MAX · PP

구간 통계값 · 최소/최대 도달 시점 측정

```
+ {AVG|MIN|MAX|PP|RMS} out
+ <FROM=val> <TO=val>
```

PARAM

전역 파라미터·측정 변수를 이용한 수식 계산

```
+ PARAM {expression}
```

주요 옵션

TD
지정 시간 경과 후 측정 시작 (TRAN)

AT = val
특정 시간·주파수·DC 값에서 측정

FROM / TO
측정 구간 제한

CROSS · RISE · FALL
n번째 교차·상승·하강 이벤트에서 측정

LAST
마지막 이벤트에서 측정 (예약어)

측정 결과 …\<proj_name>-PSpiceFiles\<design_folder>\tran 폴더에 텍스트 파일로 생성 · NUMDGT 최대 10 설정 시 정밀값 확인

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Support for .MEASURE Command

.MEASURE 버전별 지원 확대

PSpice 24.1

.MEASURE 명령어 도입

후처리 없이 시뮬레이션 중 측정

특징

- 사용자 정의 측정식으로 회로의 전기적 사양 계산
- 시뮬레이션 완료 시점에 결과를 텍스트로 생성

command를 실행하는 방법

1. `.inc` 파일로 저장 → Simulation Settings에서 Include
2. Place 메뉴로 회로도에 `@PSpice:` 텍스트 배치

PSpice 25.1

수식 기반 측정 강화

노드 전압 · 전류를 포함한 수식 지원

Sweep 확장 모델 스윕 외 추가 지원

Voltage | Current | Global Parameter | Temperature

예제 Gate 10% 상승 → Drain 90% 하강까지의 시간

```
.MEAS tdon
+ TRIG V(U1:g) VAL={vg*0.1} TD 22u RISE=1
+ TARG V(U1:d) VAL={vd*0.9} TD 22u FALL=1
```

결과 `tdon: 7.9516E-09` FROM 2.5001E-05 TO 2.5009E-05

24.1 .MEASURE 도입 → 25.1 전압·전류 수식 측정 및 Sweep 확장

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What's New in Allegro X PCB Editor & IC Packaging

박 예 솔
(Verity Technology Korea)



What's New in Allegro X PCB Editor & IC Packaging

Verity Techology Korea 박예솔 대리

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- New Structure Menu: Parameterized Structures
- Daisy Chain Enhancements
- Metal Density Scan Enhancements
- Improved Shape Performance with Dynamic Mode
- Search Panel Enhancements
- 3DX Canvas Enhancements
- Enhanced Bend Management for Flex and Rigid-Flex Designs
- ECAD-MCAD Collaboration
- New License Type: UHD (User-Host-Display)

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Migrating Designs and Supported Versions

Supported Versions

V26.1 License

V17.2 V17.4 V22.1

V23.1 V24.1 V25.1

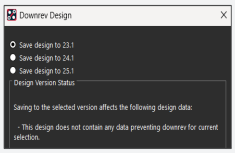
End of Support Version

Save Format

Old Version → Save in V26.1 → V26.1 Database Format

Down Revision

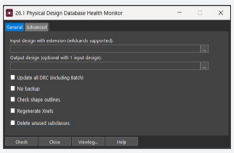
V26.1 Old Version



File > Export > Dowrev Design

Up Revision

V26.1 Old Version



PCB DB Doctor 26.1

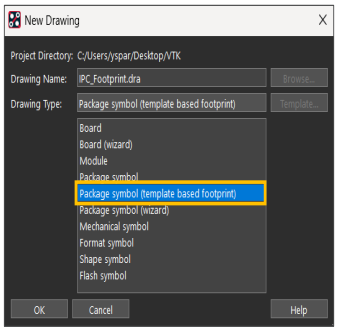
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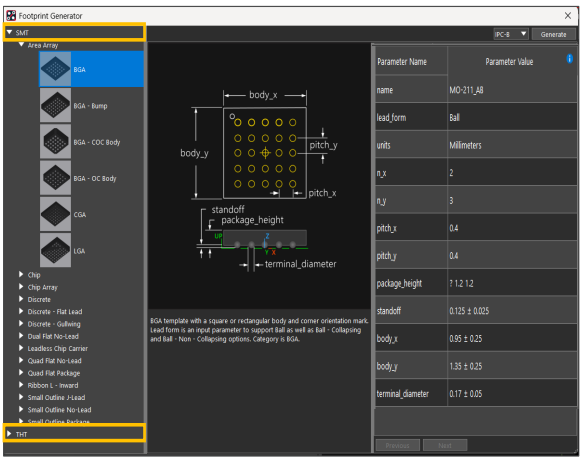
IPC-Compliant Footprints From Templates in Symbol Editor

IPC 규격 기반의 Template을 통한 자동 Footprint 생성

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Only Allegro X

- SMT 및 THP 부품 타입별 다양한 Template 항목 제공
- Parameter 설정 가능 (Pad Size, Pin Pitch, Footprint Height, Unit 등)





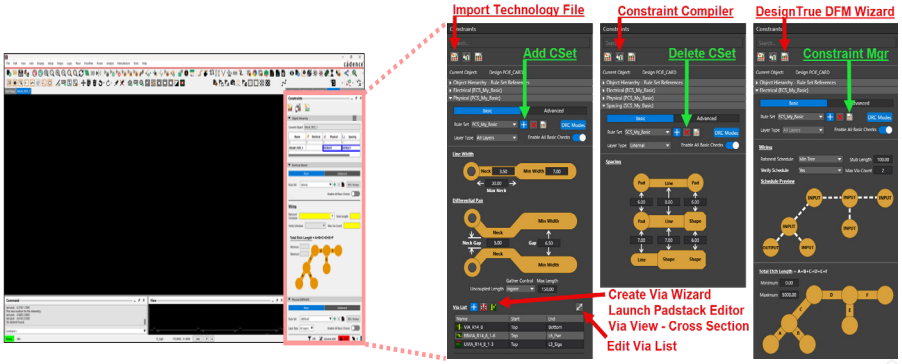
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V25.1 Update [Constraints Panel]

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New Control Panel

- Layout UI Docked Constraints Panel 도입 (Basic Mode/Advanced Mode)
  - Create CSet / Edit CSet
- Constraints 외에 Quick Access 제공
  - DFM Wizard / Constraint Compiler / Padstack Editor
  - Create Via Wizard / Cross-Sectional View of Vias / Technology File Import



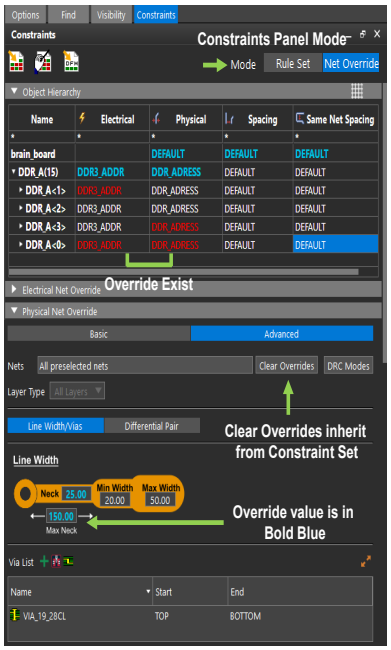
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Net-Level Overrides in Constraints Panel

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Constraints Panel New Mode: Net Override

- Constraints Panel Mode
  - Rule Set: CSet 기반의 Design Rule 관리
  - Net Override: Net 단위의 Design Rule 관리
- Override 식별 색상
  - Override 발생 Net: CSet 설정값과 상이할 경우 Bold Red로 표시
  - Override 적용: 변경한 Net Rule은 Bold Blue로 표시

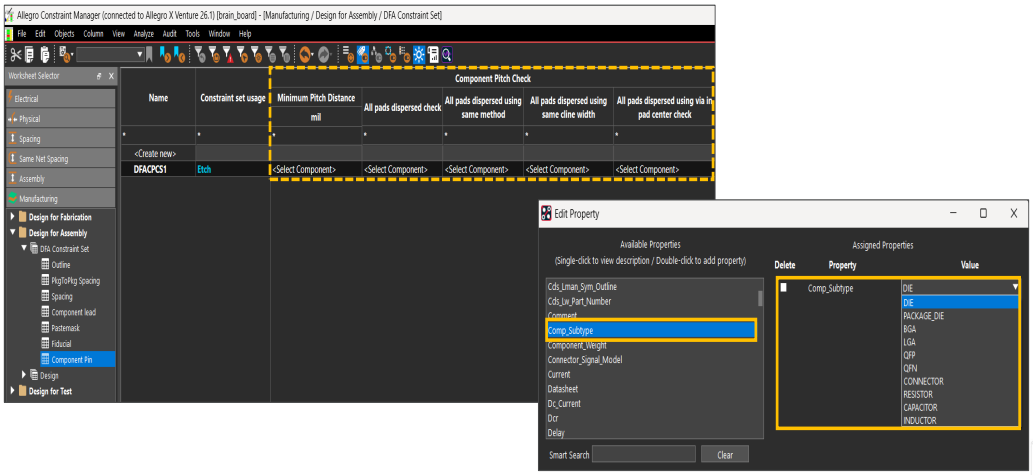


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Component-Level Design for Assembly Checks

- BGA 등 High-Density Packaging의 Escape Routing 및 Fan-out Pattern을 검증하는 DFA Rule
- Manufacturing > Design For Assembly > “Component Pin”
- [COMP_SUBTYPE] 부품 속성 정의 필요

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Allegro X Venture
Allegro X APD Layout

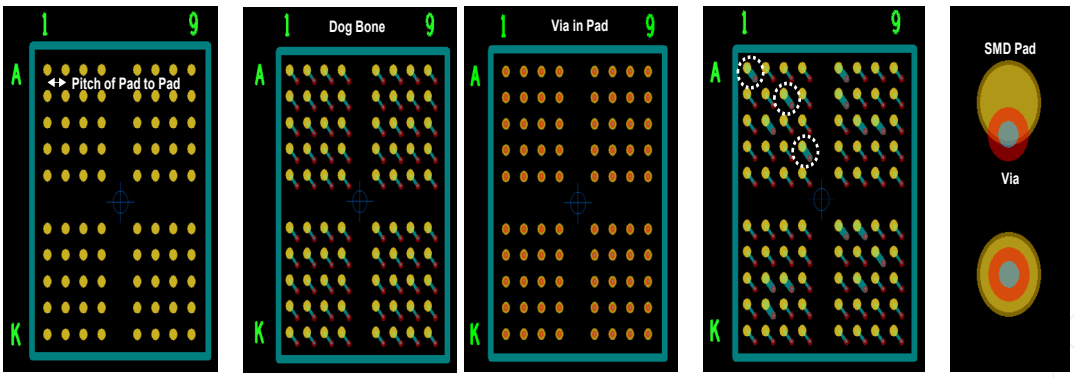


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Component-Level Design for Assembly Checks

Name	Constraint set usage	Component Pitch Check				
		Minimum Pitch Distance (mil)	All pads dispersed check	All pads dispersed using same method	All pads dispersed using same cline width	All pads dispersed using via in pad center check
*	*	*	*	*	*	*
<Create new>						

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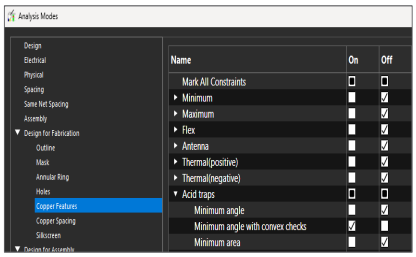
Usability Enhancements

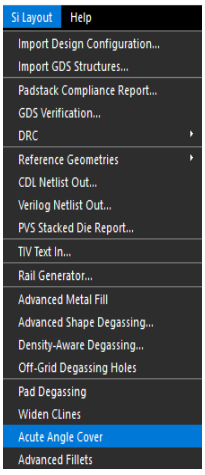
DFM Acute Angle Cover Check Support

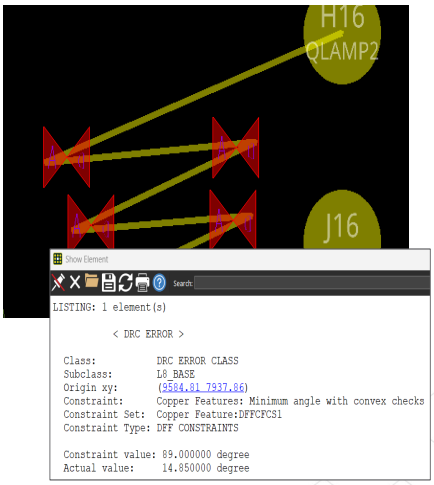
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Allegro X APD Enterprise
Allegro X APD Expert
Allegro X Silicon Layout Option

- DFM DRC: Acute Angle 자동 식별
- Si Layout > Acute Angle Cover: Acute Angle Cover DRC Solution







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V25.1 Update [Manage Topology-Based Electrical Constraint Sets with Topology Workbench]

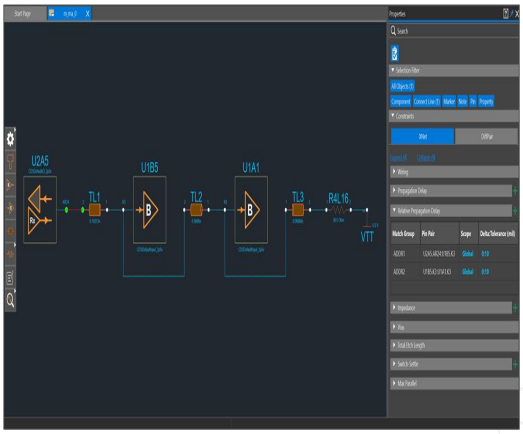
- 기존 Signal Explorer 보다 향상된 UI와 단순한 사용 구조를 갖추고 Topology 기반 Electrical Rule을 더 쉽게 관리
- 복잡한 Pin Pair, BUS 설계에서도 Electrical Rule Generate 시간 단축

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OrCAD X Professional
Allegro X Advanced Package



Signal Explorer



NEW: Topology Workbench

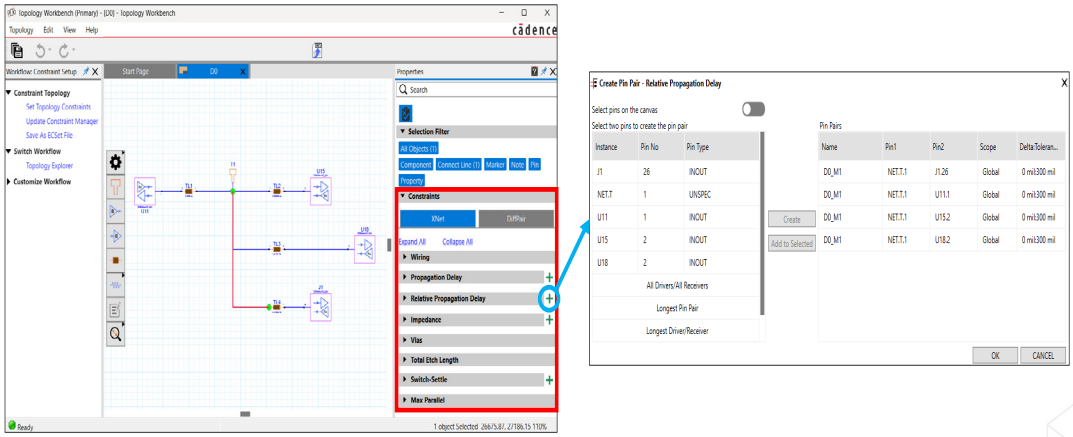
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V25.1 Update [Topology Workbench – Constraint]

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- Topology에 적용할 Electrical Constraint를 정의하는 영역
- 선택한 Wire 또는 Pin Pair에 대해 Propagation Delay, Relative Propagation Delay, Impedance, Total Etch Length Rule 설정



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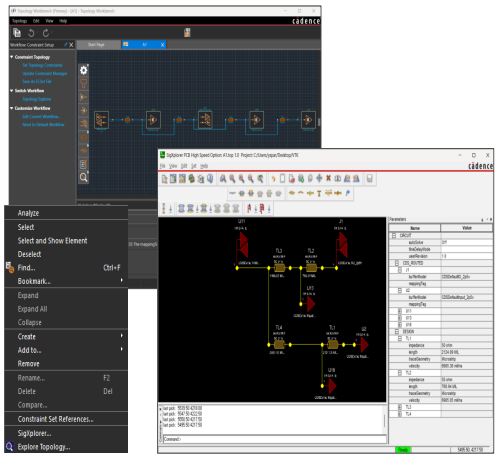
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Use Topology Workbench for Electrical Constraint Topologies

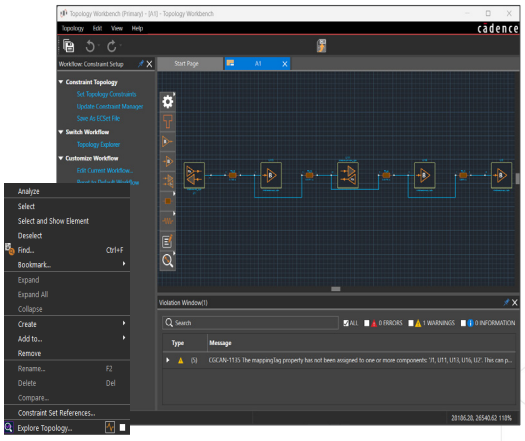
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Allegro X Advanced Package

Topology Workbench 통합

- Old Version: Signal Explorer 기반의 토폴로지 구성 및 시뮬레이션
- V26.1: Signal Explorer 지원 종료 → Topology Workbench 기본 적용



Old Version



V26.1

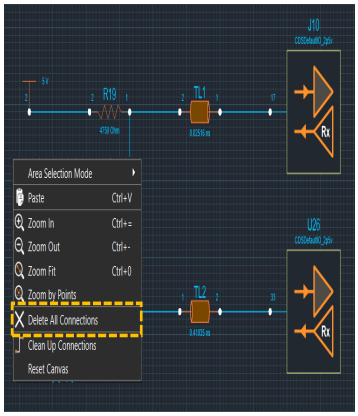
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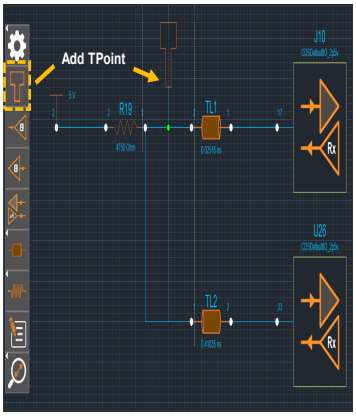
Use Topology Workbench for Electrical Constraint Topologies

Topology Workbench Improvements

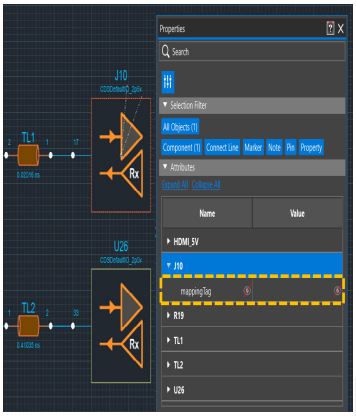
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Delete All Connections



Add TPoint



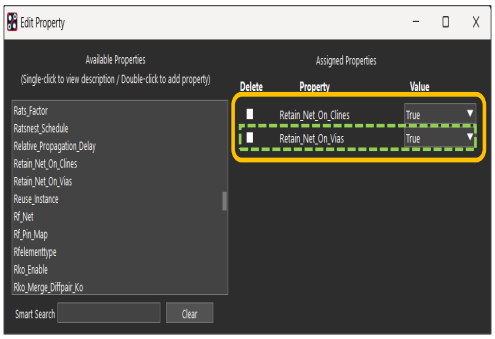
Mapping Tag

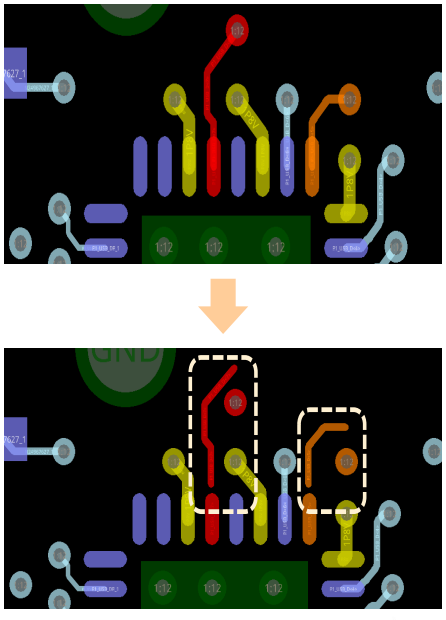
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Property to Preserve Net Assignments Added

배선 Net 할당 유지 속성 추가

- Old Version: Retain Net on Vias (Via의 Net 속성만 유지 지원)
- V26.1: Retain Net on Clines 추가 지원





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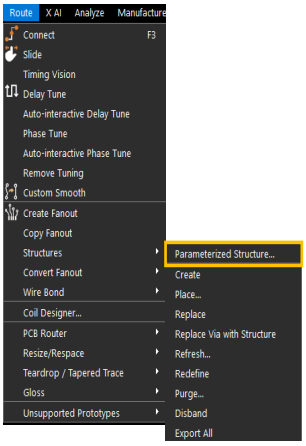
High-Speed Parameterized Structures

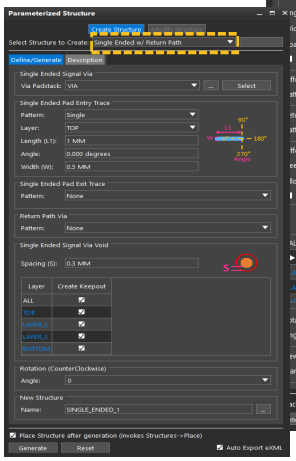
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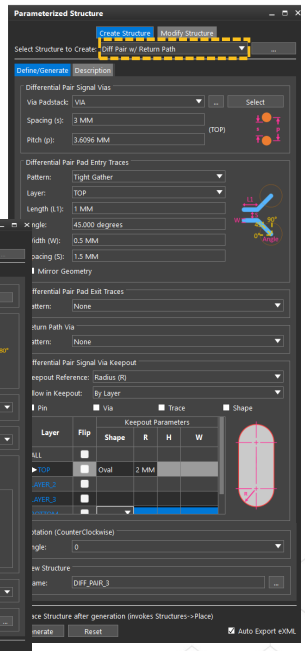
Allegro X Designer Plus
Allegro X APD Layout

New Structure Menu: Parameterized Structures

- Supports creating and editing parameterized structures in the Parameterized Structures Panel
- Parameterized Structures Type: Differential-pair / Single-ended
- Set parameter: Return-path via, Entry/Exit trace, Signal-via keepout







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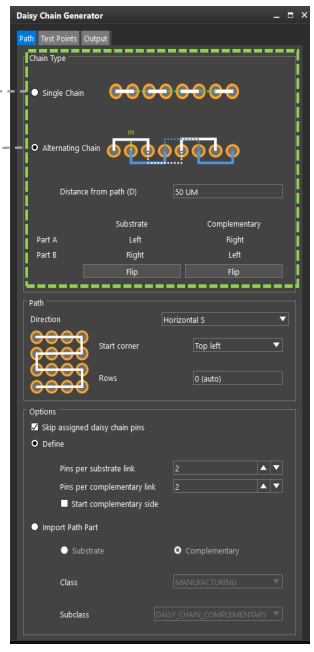
Daisy Chain Enhancements

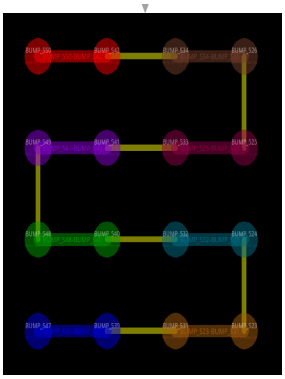
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Allegro X APD Layout

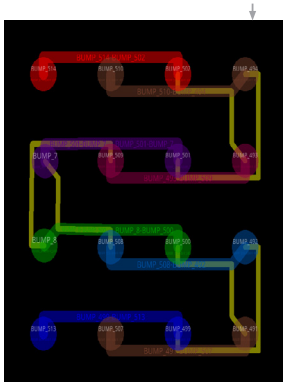
Daisy Chain Generator New Chain Type

- Old Version: Path / Option만 존재
- V26.1: Chane Type 생성 (Single Chain / Alternating Chain)





Single Chain



Alternating Chain

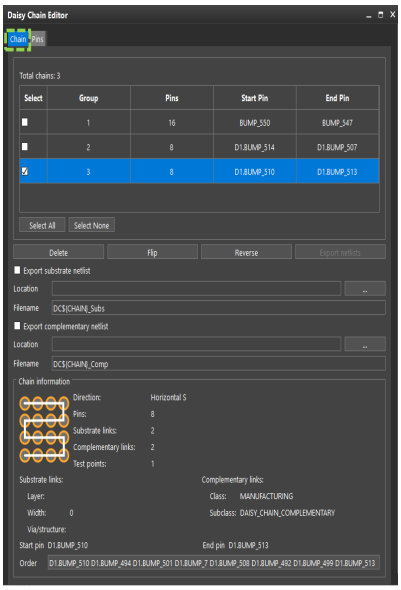
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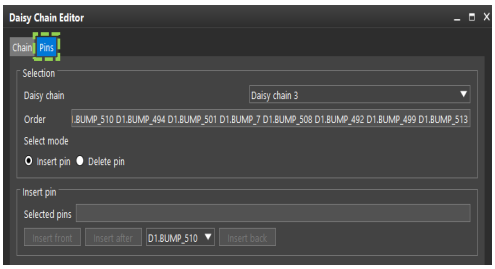
Daisy Chain Enhancements

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Allegro X APD Layout

Daisy Chain Editor

- 구성된 Daisy Chain의 전체 구조 및 시작/종료 Pin 확인
- Chain 내 특정 Pin의 Insert 및 Delete 기능 제공
- 불필요한 Daisy Chain 구조 자체 Delete 및 관리



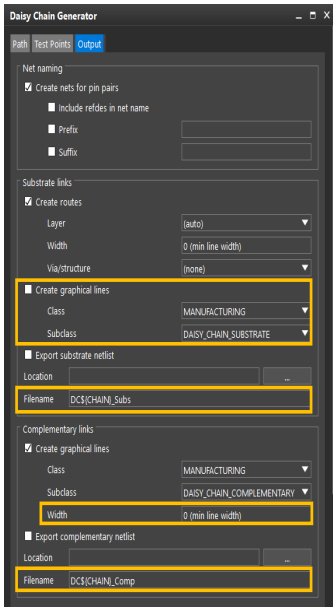


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Daisy Chain Enhancements

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Daisy Chain Generator New Option



Additional usability enhancements include:

- Exporting netlist for all daisy chains
- Assigning a name to the netlist file
- Selecting graphical chain lines on the substrate
- Configuring complementary-link line width
- Highlighting full-chain

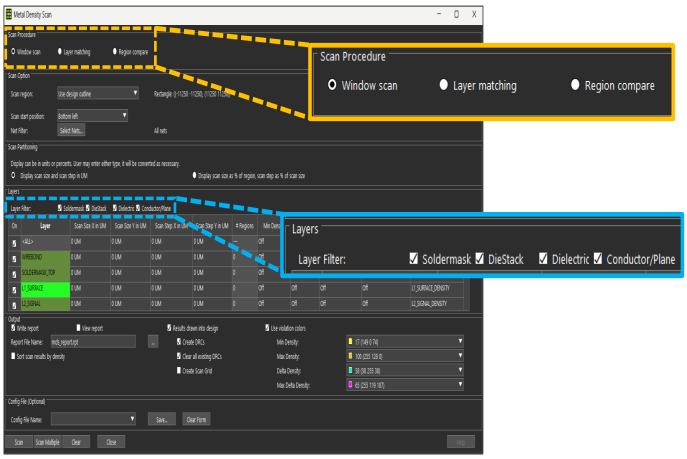
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Metal Density Scan Enhancements

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Allegro X APD Layout

Metal Density Scan New Option

- Scan Procedure: Window scan, Layer matching, Region compare
- Layer Filter 추가: Soldermask, DieStack, Dielectric, Conductor/Plane

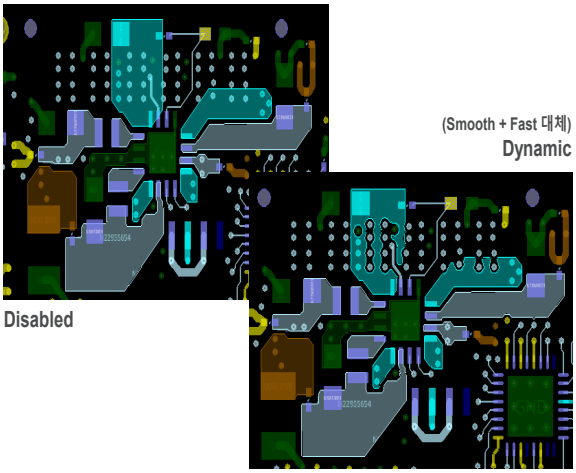


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Improved Shape Performance with Dynamic Mode

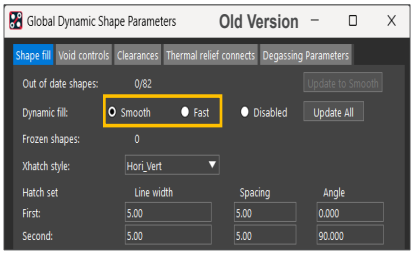
Shape Type 통일화

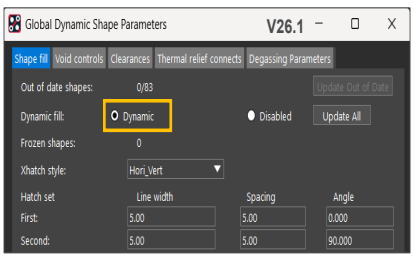
- Old Version: Shape Fill Mode 분리 (Smooth / Fast / Disabled)
- V26.1: Shape Fill Mode 통합 (Dynamic / Disabled)



Disabled

(Smooth + Fast 대체)
Dynamic



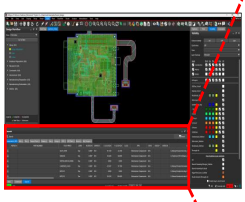


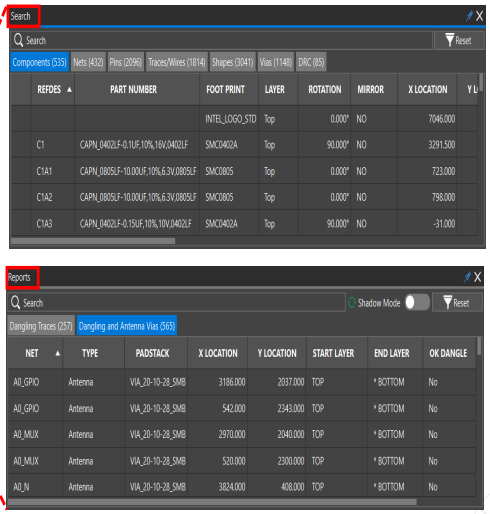
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V25.1 Update [Docked Informational Panels]

Search Panel

- Object Search / Select
- Search Panel → Layout 간 Probing 가능
- Real-Time Updates





Report Panel

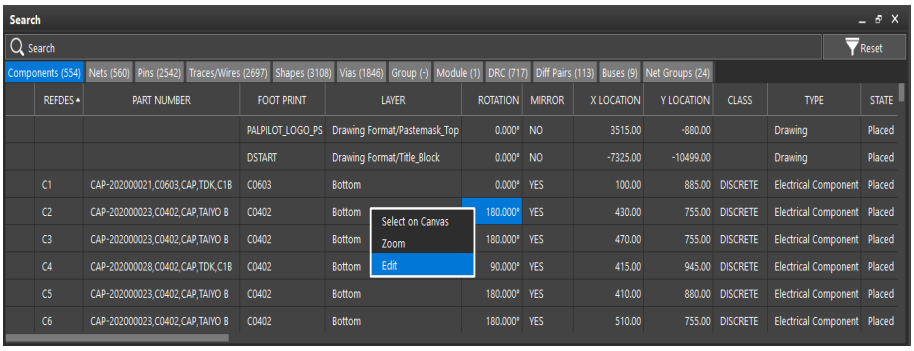
- Shape Islands Report
- Unassigned Shapes Report
- Missing Teardrops Report
- Missing Tapers Report
- Dangling Traces, Vias, and Antenna Report

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Search Panel Enhancements

Modify Object Properties from Search Results

- Search Panel에서 검색된 객체의 속성을 편집할 수 있도록 기능 향상
- Parameter 변경 시 Layout 상에 실시간으로 반영
- Old Version: 단순 디자인 정보 확인 Viewer → V26.1: 실시간 데이터 수정이 가능한 Interactive Edit Panel로 개선

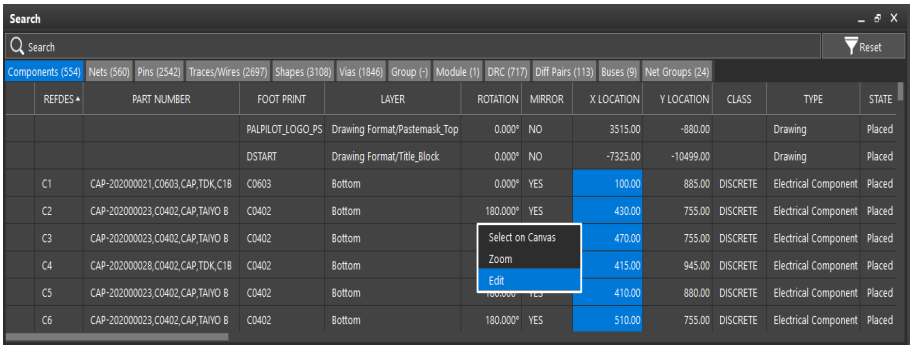


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Search Panel Enhancements

Update Multiple Objects Simultaneously

- Search Panel 내 복수 객체 선택 및 동일 속성 일괄 수정 지원
- 여러 부품의 Rotation 값 등 동일 속성을 단 한 번의 작업으로 동시 업데이트

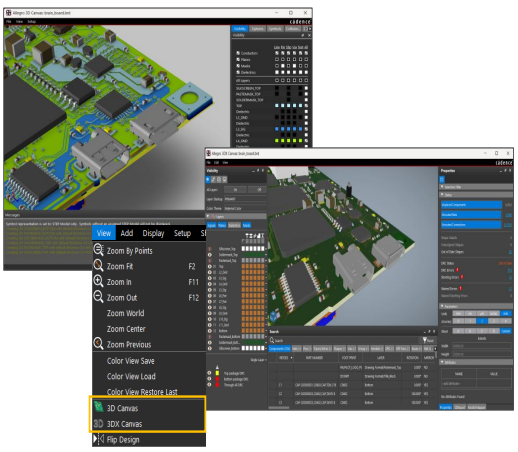


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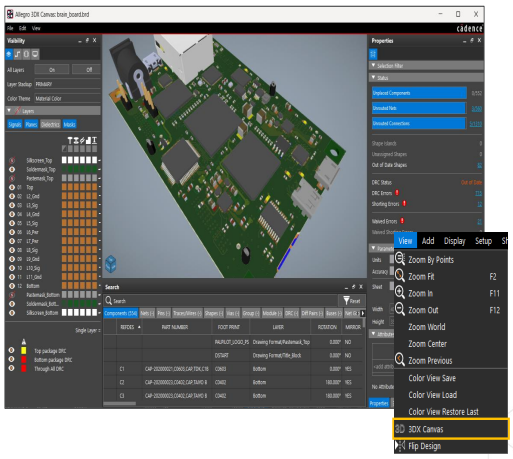
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3DX Canvas Enhancements

- 기존 3D Canvas ➔ 차세대 3DX Canvas 전용 플랫폼으로 통합
- 주요 향상 기능:
  - Enhanced Bend Management for Flex and Rigid-Flex Designs



Old Version



V26.1

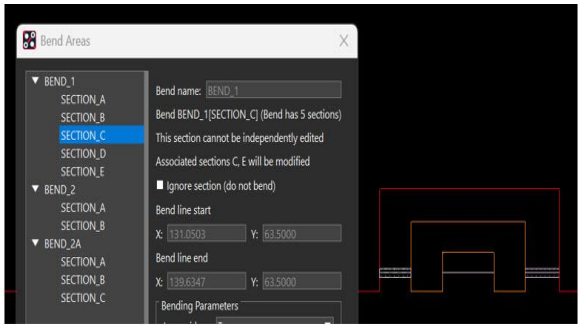
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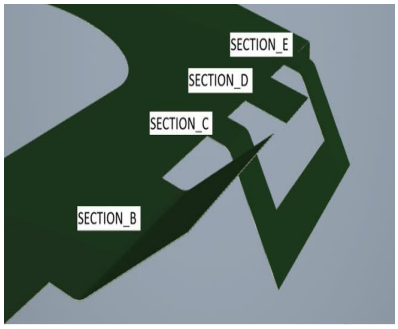
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Enhanced Bend Management for Flex and Rigid-Flex Designs

Flex 및 Rigid-Flex Bend 관리 기능 통합

- Manage Bends 설정 통합: Flex/Rigid-flex Bend Create & Edit Workflow 통합
- 복잡한 Bend 지원 및 표준: Multi-Section Compound Bend 지원 및 IDX V6 표준 대응



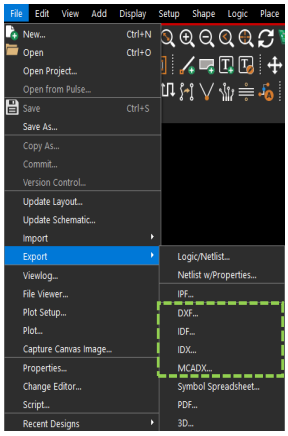


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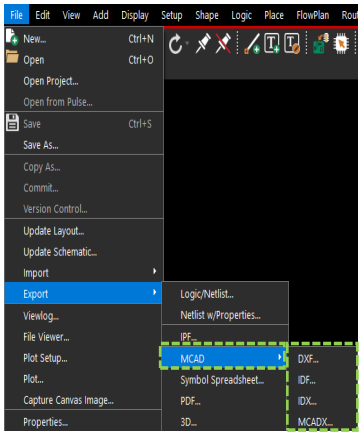
ECAD-MCAD Collaboration

ECAD-MCAD 메뉴 통합 및 Workflow 간소화

- Export 내 MCAD 통합 메뉴: DXF, IDF, IDX, MCADX 등 MCAD Date Format을 한곳으로 통합
- Import/Export 경로를 단일화하여 MCAD 변환 작업 효율 향상



Old Version



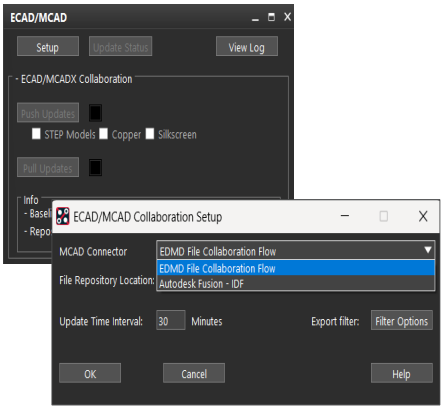
V26.1

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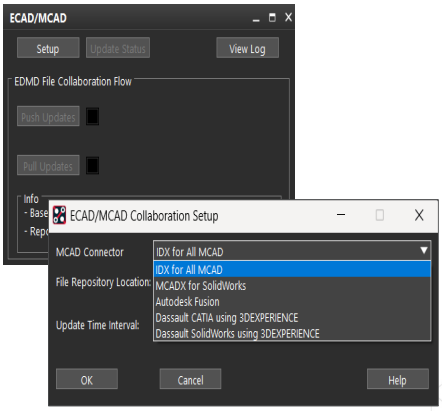
ECAD-MCAD Collaboration

ECAD/MCAD Collaboration 설정 및 Connector 목록 개선

- 사용 가능한 Co-design Workflow 옵션을 명확히 구분하여 선택 절차 단순화
- IDX for All MCAD, MCADX SolidWorks, Autodesk Fusion 등 주요 MCAD 별 Option 지원



Old Version



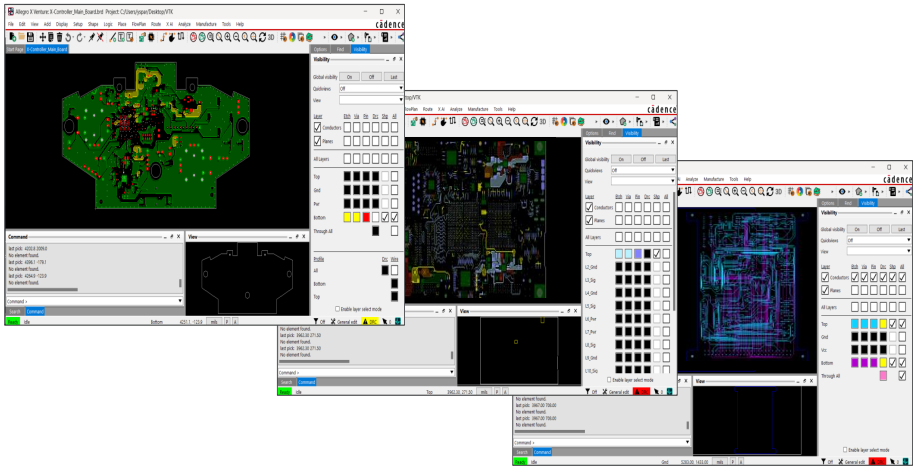
V26.1

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New Licenses Type

New License Type: UHD (User-Host-Display)

- PC 1: Running multiple instances of Allegro X Layout ⇒ Check out 1 license at no additional license cost
- PC 1, PC 2...: Running multiple instances of Allegro X Layout simultaneously on different PCs ⇒ Per PC Individual License Check Out



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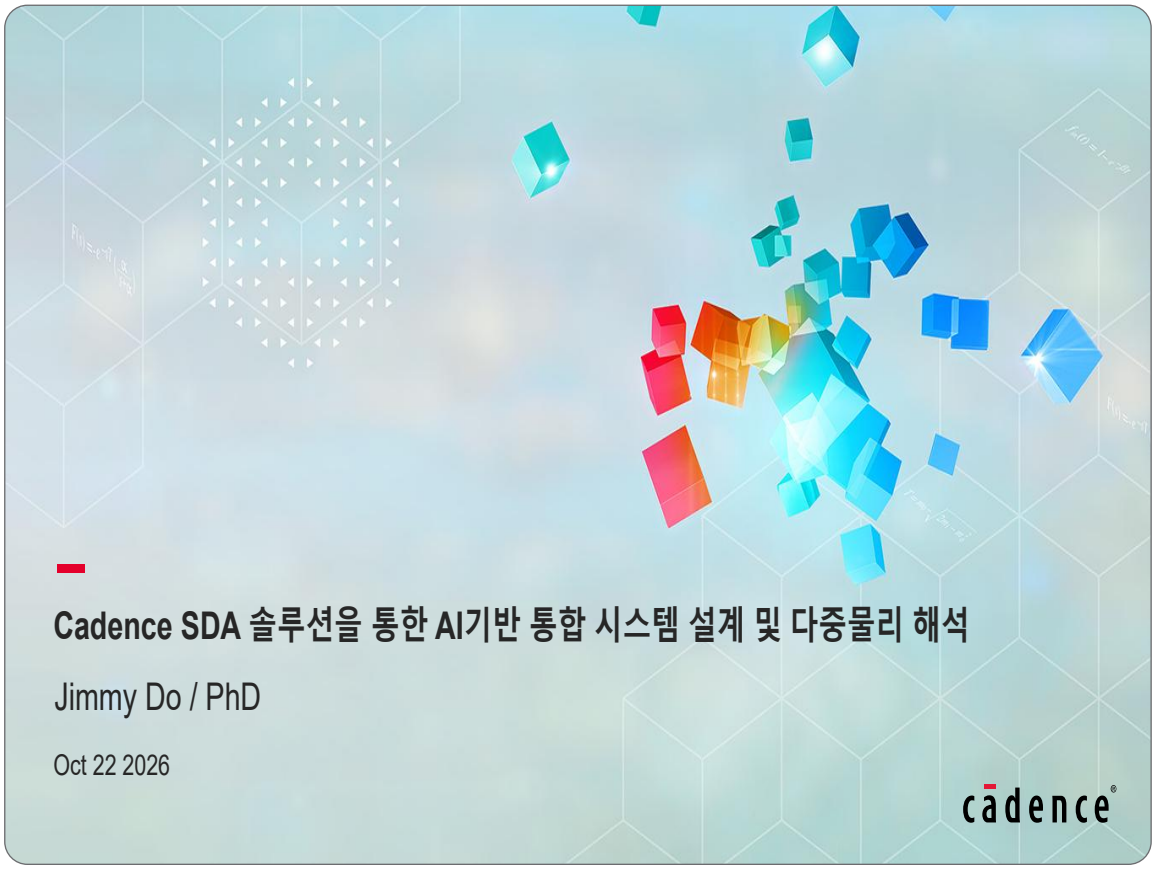
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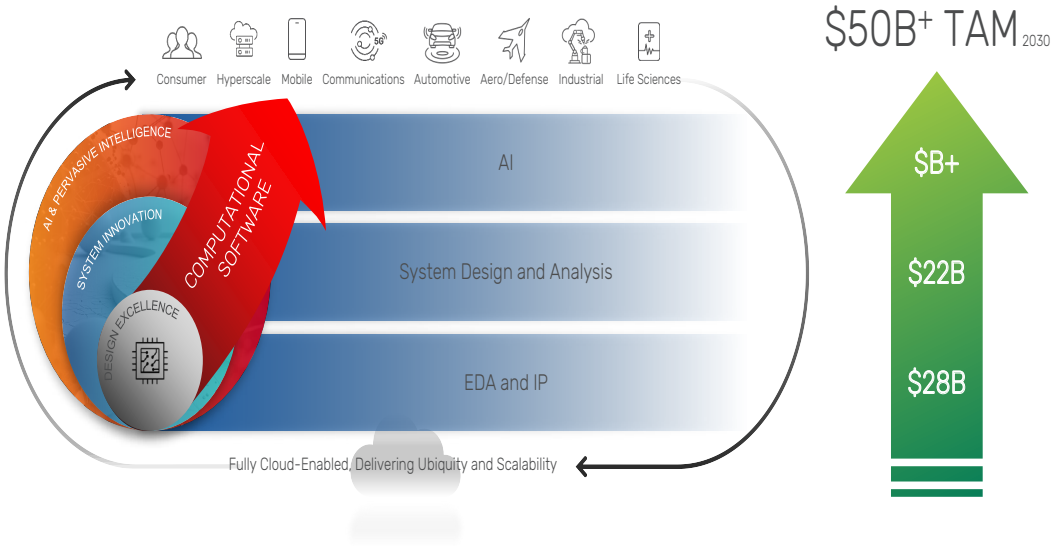
Cadence SDA 솔루션을 통한 AI기반 통합 시스템 설계 및 다중물리 해석

도 지 훈
(Cadence Korea)


Cadence SDA 솔루션을 통한 AI기반 통합 시스템 설계 및 다중물리 해석
Jimmy Do / PhD
Oct 22 2026
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Systems Design and Analysis
Overview
2
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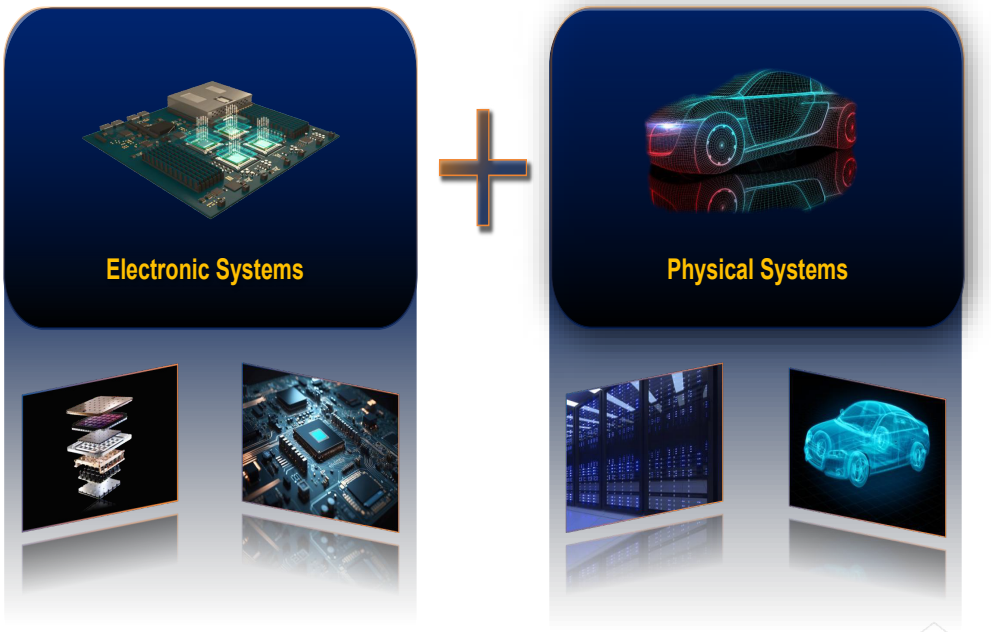
Cadence Intelligent System Design Strategy



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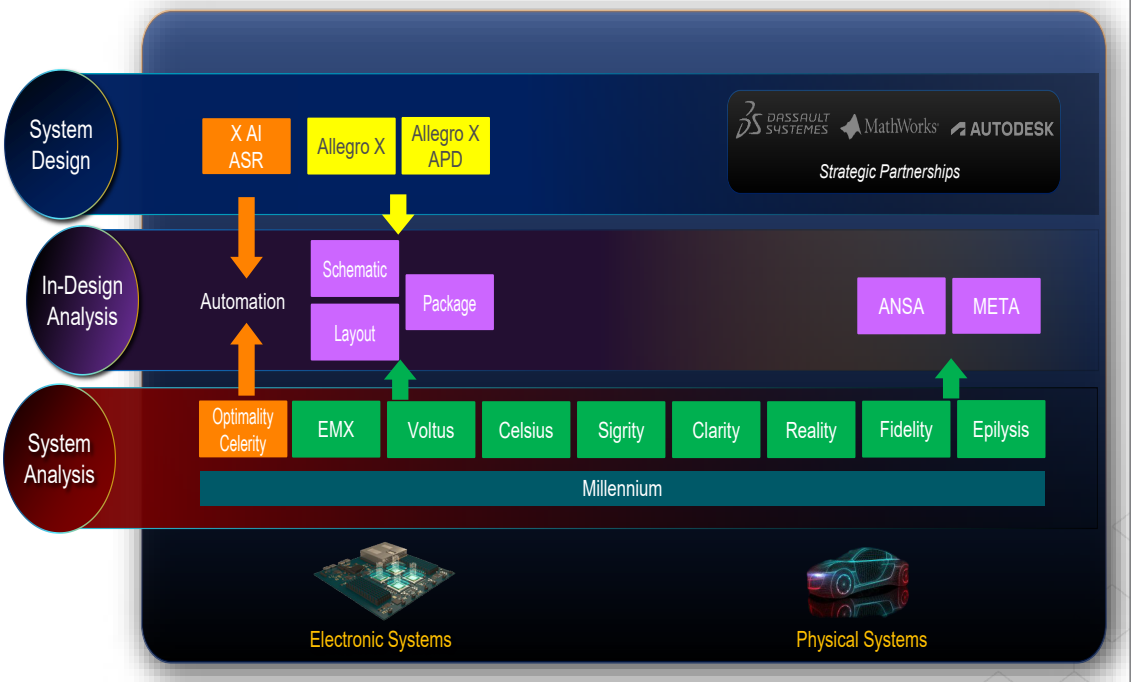
Cadence Systems Focus



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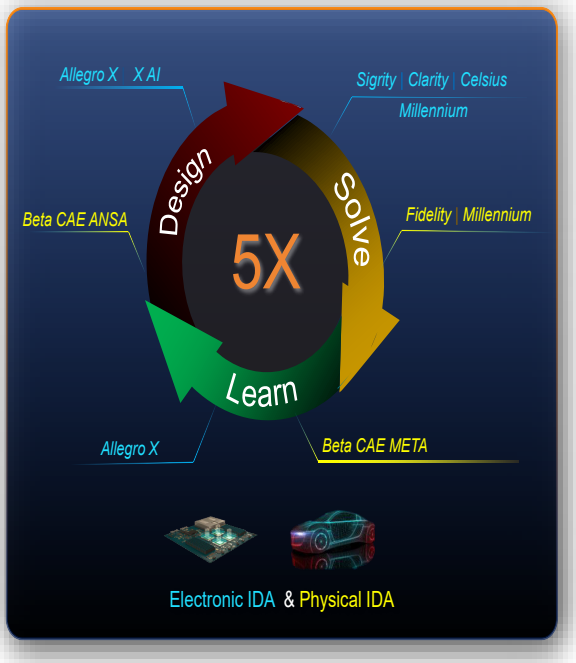
System Design & Analysis Platform



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In Design Analysis Flows

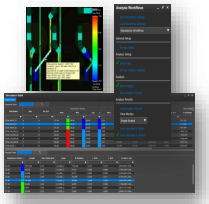


- IDA is at intersection of design & analysis
  - Electronic AND Physical Systems
  - Design, Solve, Learn iteration has huge impact on design TAT
  - Enables early identification of problems
- Key reason why we acquired Beta
  - "Physical IDA" enablement
  - Applications to Electronic IDA too
- Our Focus: Enable fastest, most productive iterations → reduce TAT

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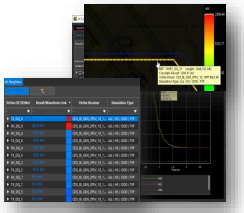
Example of Allegro X & Sigrity X In Design Analysis



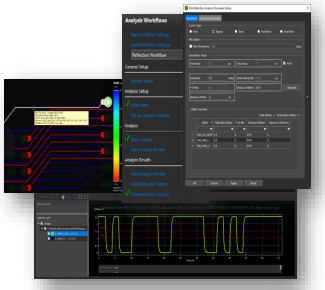
Impedance Analysis Screening



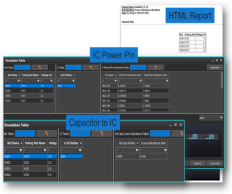
Coupling Analysis Screening



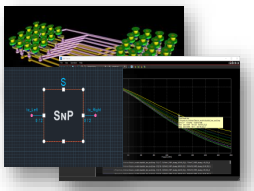
Crosstalk Analysis



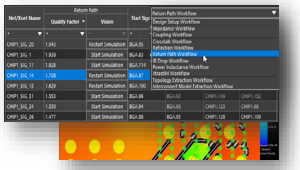
Reflection Analysis



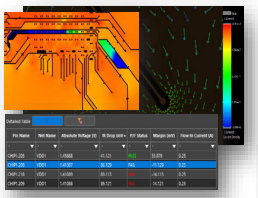
Power Inductance Analysis



Interconnect Model Extraction (IME)



Return Path Analysis

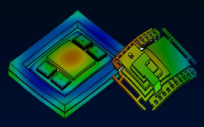
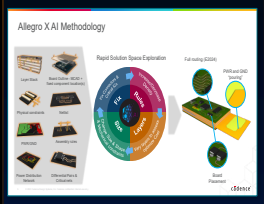
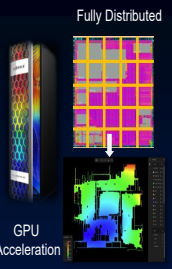


IR Drop Analysis

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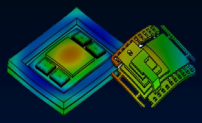
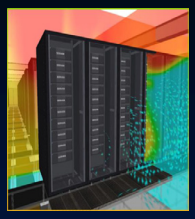
Selected 2026 Highlights

Warpage Analysis	Allegro X AI	Allegro X APD Advanced Substrate Router	Voltus Infinity
			
Critical Reliability Consideration for HBMs, 3DIC, Packaging	PCB P&R Automation On-prem solution EA 2025	Industry's Only Partner success : AMD and TSMC	Very Large-Scale EMIR 10X faster, GPU acceleration, new UI

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Recent Highlights & Upcoming Roadmap Items

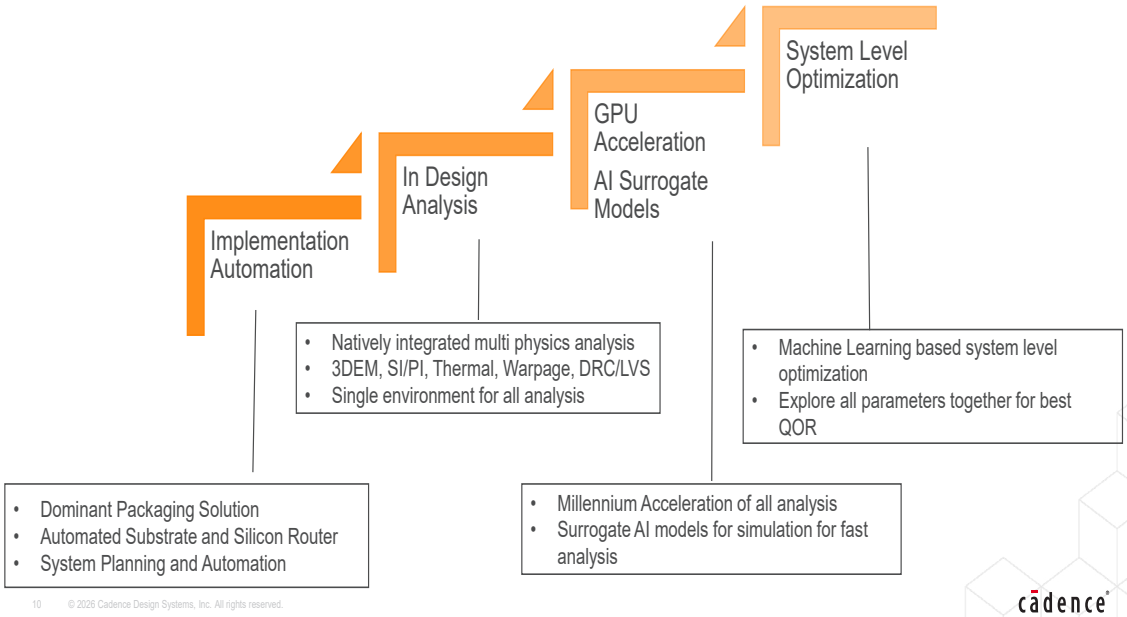
Millennium	Warpage Analysis	Beta CAE + Fidelity IDA	Reality DC Insight
			
GPU Acceleration New: Voltus, Clarity, Celsius, Warpage	Critical Reliability Consideration for HBMs, 3DIC, Packaging	In-Design CFD Workflow (Refine, Solve, Learn) Accelerated Design/Decisions	Optimize Data Center Design & Operations Embedded Multiphysics Analysis

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System Design Automation and Optimization

Four step ladder to fully optimized solutions



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AI and Automation in SDA

IC Packaging, PCB and Multiphysics

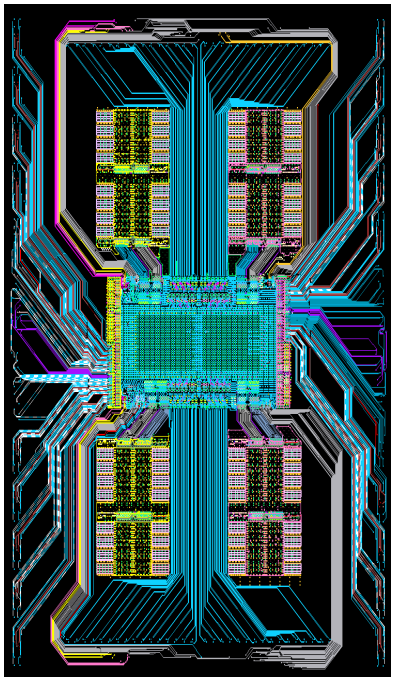
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Advanced Substrate Router (ASR)

For Packaging and PCB

- The bottleneck for advanced package design is ROUTING
- Optimized for routing high density Die to Die & Die to Substrate connections, multi-core performance benefits
  - 9 die D2S/D2D design takes ~55 min (4 cores)
- Supports diverse requirements
  - Any angle routing, auto shielding, bus breakout routing
  - High density bump escape planning, differential pair routing
  - Fillet/teardrop insertion for yield improvement
- Featured at TSMC OIP
  - Only substrate router green-dot
  - Joint presentation with AMD
- What's next: route feasibility
  - Congestion maps, creating and routing bundles, PTH via placement
- Advanced Packaging now, PCB next…



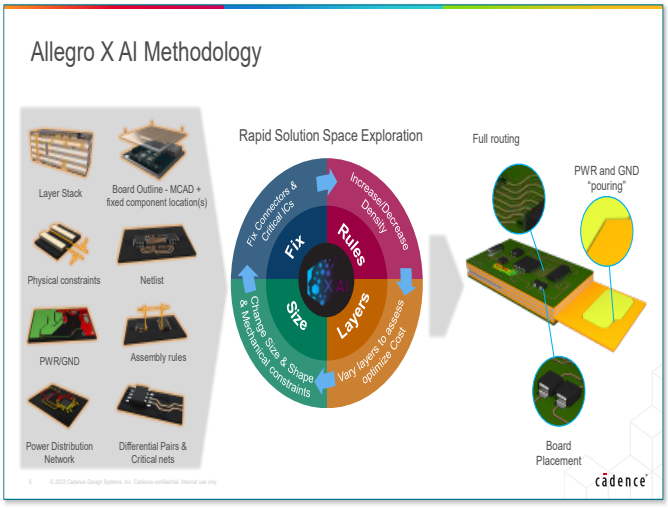
ASR routed – 9 die D2S/D2D design

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X AI Methodology and Roadmap

Upfront constraint definition enables automation & design exploration



Recent Highlights

User workflow improvements for EoU

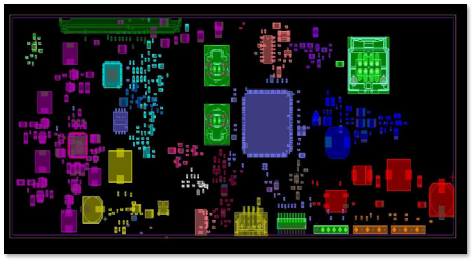
Significantly improved placement quality

ASR for PCB

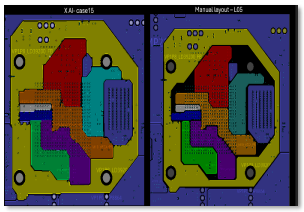
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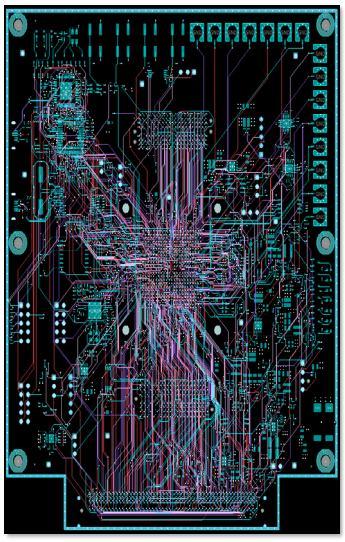
X AI/Automation Technologies



PCB Placement



PCB PG "Metal Pouring"



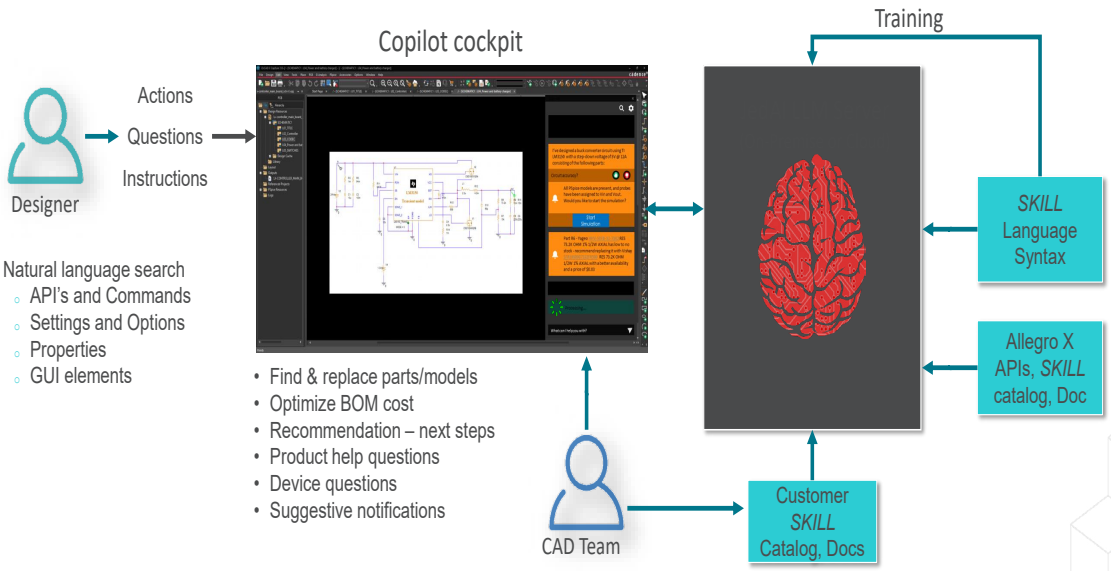
Early PCB Routing (~700 nets, 5 min)

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Generative AI – System CoPilot

Native LLM Within Allegro X



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MSA CoPilot

Portfolio: Voltus, Celsius, Clarity, Sigrity, Reality, Fidelity, Beta CAE

Simulation Setup	Auto Report Generation	Natural Language Queries	Root Cause Analysis	Performance Review
• Drive tools and functions	• Generates reports from design and analysis data	• Q&A search/ documentation	• Identifies issues	• Offers recommendations • Applies fixes, re-solves and reports

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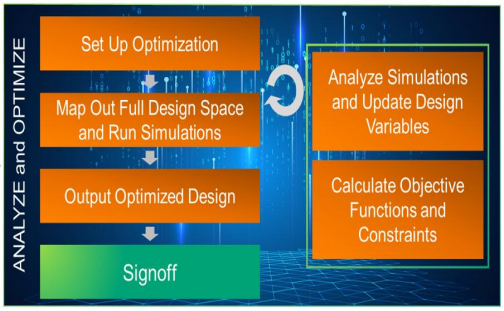
Optimality AI Automation

Reduces time to produce Optimized Designs

- AI-driven multiphysics optimization
- Optimize electrical performance in multiphysics simulation as a function of design variables and constraints
  - Clarity, Celsius and Sigrity
- Complete System-level exploration: chip, package, board
  - Allegro Integration

"Optimality allowed us to realize a 75% performance improvement for our recent 112G PAM4 SerDes project"

Aaron Yang and Howard Yin, Design Directors, MediaTek





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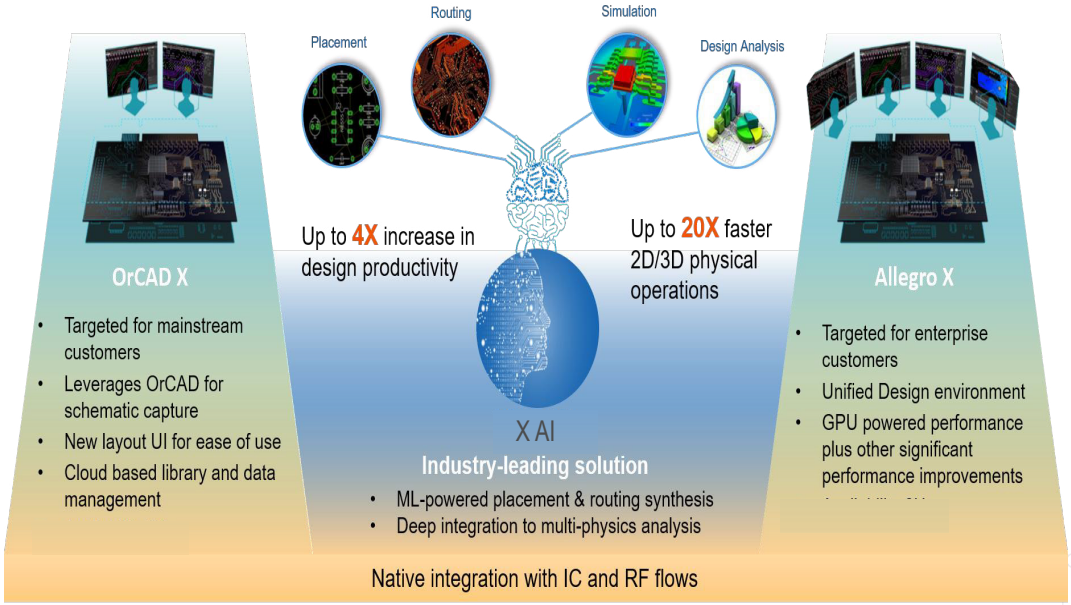


PCB Portfolio and New Technologies

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Cadence PCB Solutions

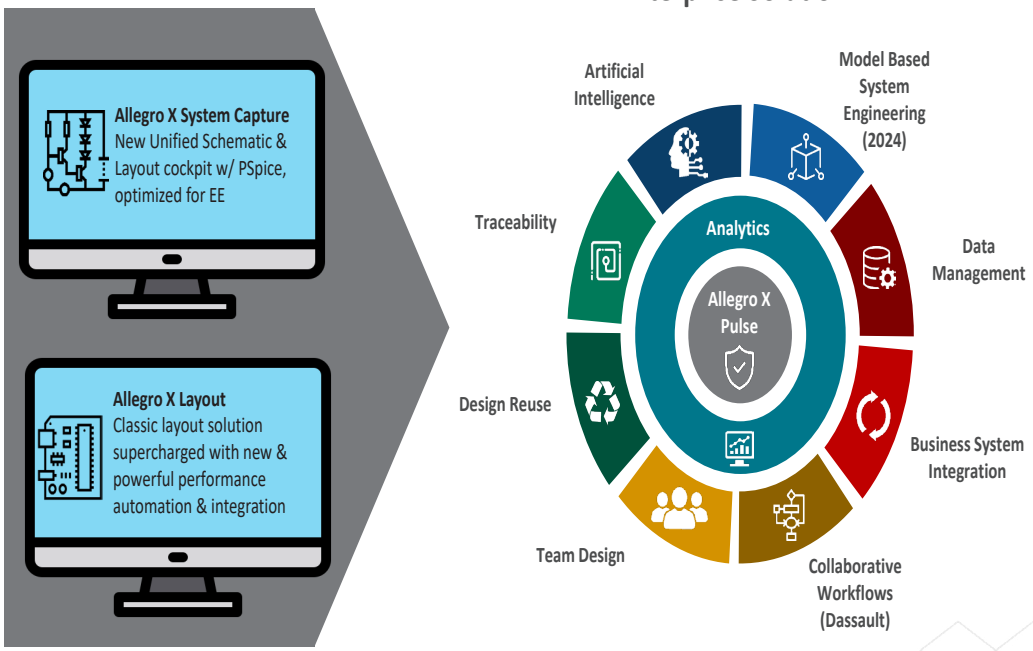


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What is Allegro X?

AllegroX

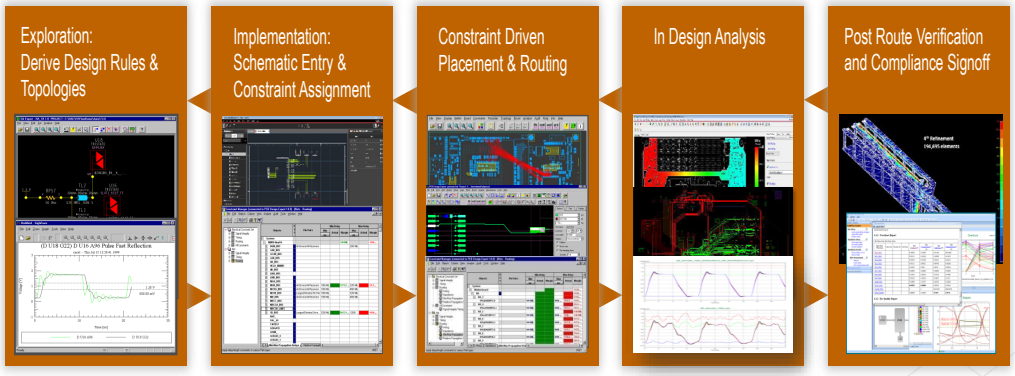


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Allegro X Constraint-Driven Design

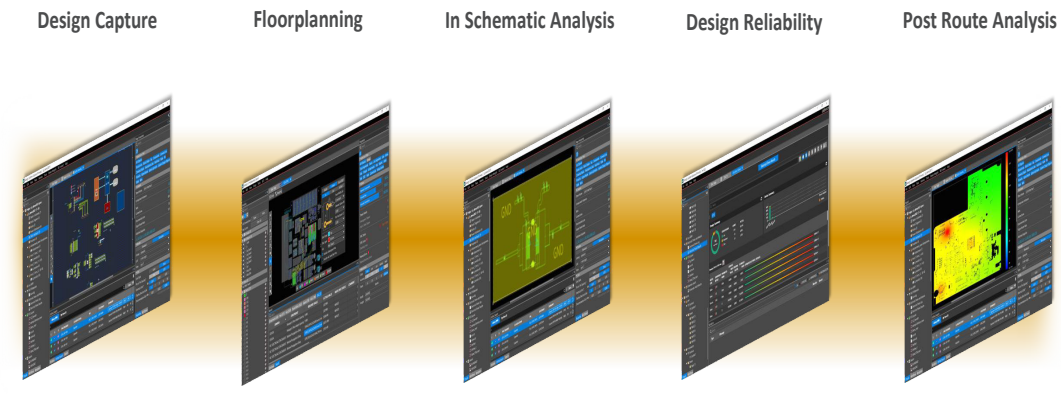
- Correct-By-Design Methodology
- Enter and Manage Constraints in Schematic or PCB Layout
- Single Constraint Environment accessed at any stage of design
- Supports IP Design Reuse and Team Design
- Allegro Constraint Compiler



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Increasing EE Productivity with Allegro X System Capture

From Schematic Capture to Convergence of Five Views in a Fully integrated EE Cockpit



System-level design (schematic and layout), FIDES reliability standard support, Schematic driven layout for X AI

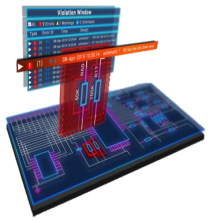
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Allegro X System Capture

Design reliability

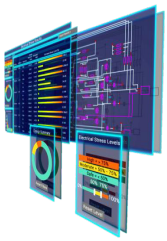
Schematic Audit

- ✓ Verify the integrity of the schematic for inadvertent mistakes
- ✓ Cross-probe to instances and nets to fix warnings and errors
- ✓ Waive acceptable violations



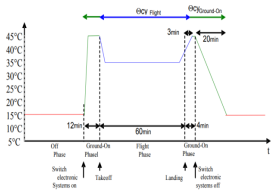
Electrical Overstress

- ✓ Verify electrical stress for each device at multiple temperatures
- ✓ Visualize stress reports with different derating
- ✓ Ability to cross-probe to a portion of the circuit impacting the device stress



Advanced Solutions

- ✓ Meantime between Failure Analysis (MTBF)
- ✓ FIDES Standard – Time-based profile predicts life expectancy
- ✓ Failure Mode Analysis (FMEA) – In Development

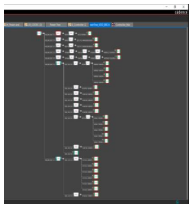


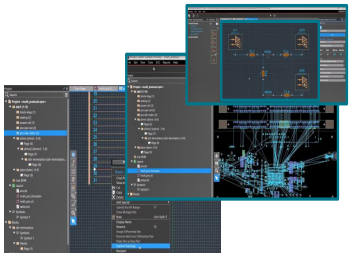
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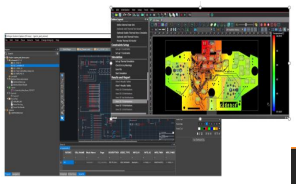
Allegro X

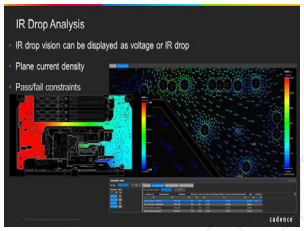
SI / PI / Thermal Analysis

- Power Topology Analyzer for early power rail assessment at the schematic level
- Sigrity™ Topology Explorer (TopXP) integration with 'schematic + floorplan' analyzes signal integrity of high-speed nets
- Celsius™ integration assesses Thermal considerations at schematic and layout
- In-Design Analysis flows finds common issues before handoff to expert
  - Impedance, Coupling, Reflection, Crosstalk, Return Path, IR Drop, Power Inductance





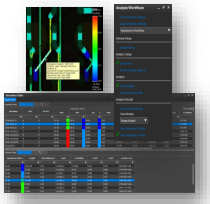




Schematic Capture → MCAD & Placement Constraints → EE Pre-layout / Exploration → **PCB Design** → **Analysis** → Signoff Analysis

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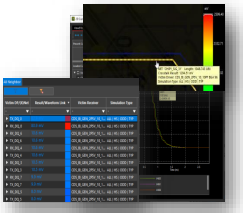
Allegro X In-Design Analysis



Impedance Analysis Screening



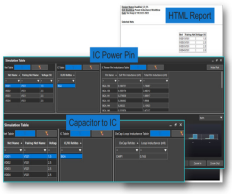
Coupling Analysis Screening



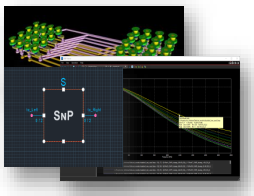
Crosstalk Analysis



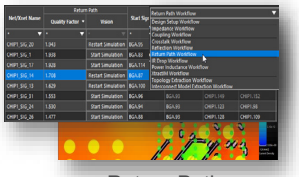
Reflection Analysis



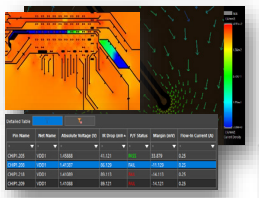
Power Inductance Analysis



Interconnect Model Extraction (IME)



Return Path Analysis



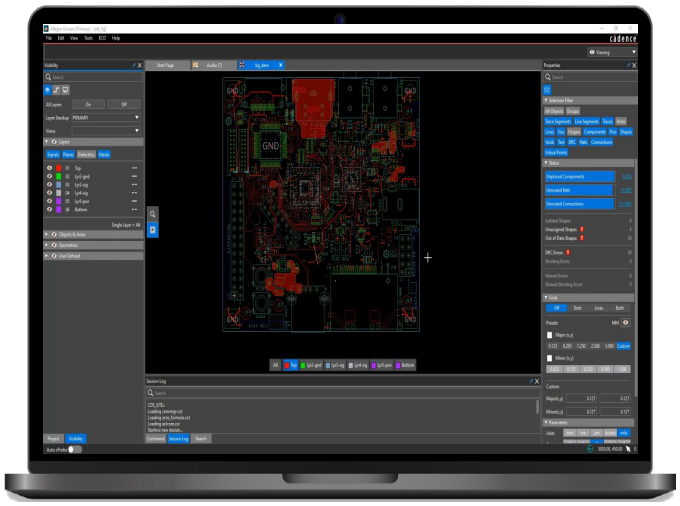
IR Drop Analysis

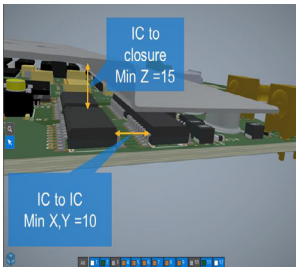
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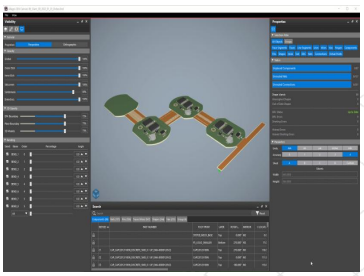
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New 3D Solution

- 40X+ increase in performance
- 10X+ improved capacity
- High-performance 3D visualization
- Real-time 3D incremental updates
- Interactive database browsing and measurement
- Interactive bending visualization
- 3D Placement DRCs





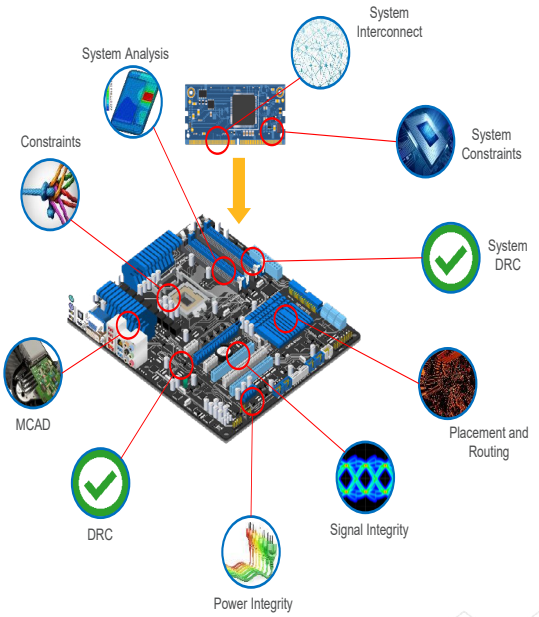


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Symphony – Multiply Your Teams Effectiveness

- Concurrent Real-time Design
  - PCB Layout
  - Package Design
  - InDesign SI & PI Analysis
  - Manufacturing Markup
  - EE Design Review
- Easy to Setup & Deploy
- No Special Hardware
- Client or Server Configuration
- Single Database
- Constraint Editing



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Expanded ECAD / MCAD Co-Design

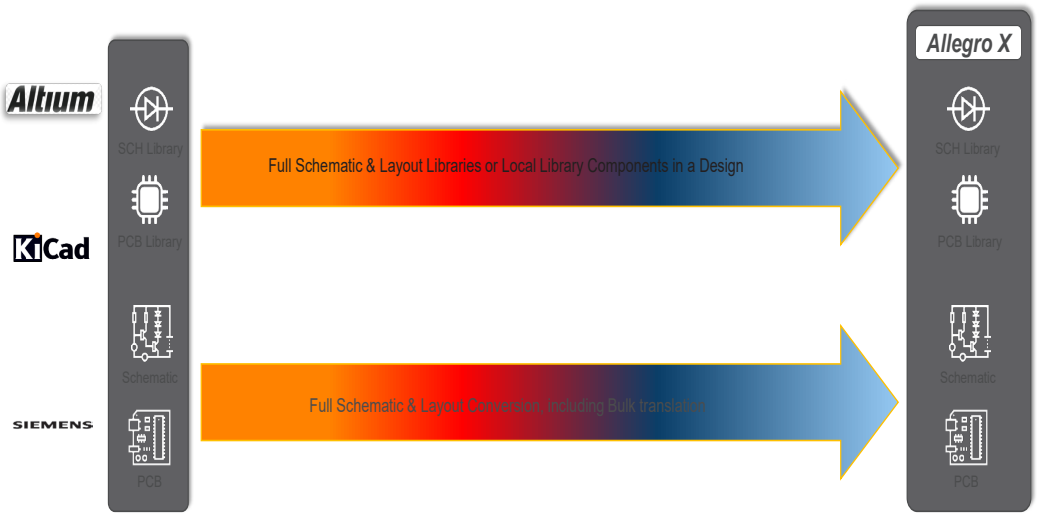
- Seamless collaboration with Dassault Solidworks
  - Robust Solidworks plug-in, installs in minutes.
- Advanced Solidworks plug-in features in development
  - Rigid/Flex bending in Solidworks
  - Skinning effect for large copper rendering in MCAD
  - Constraint Exchange
  - Multi-board design
- Cloud to Cloud integration with 3DEXPERIENCE provides out-of-the-box Publish for Manufacturing
- ADSK Fusion integration just released!
- Strong integration with Siemens NX and PTC Creo continues



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Streamlining Competitive Displacement

Key Translators in Development



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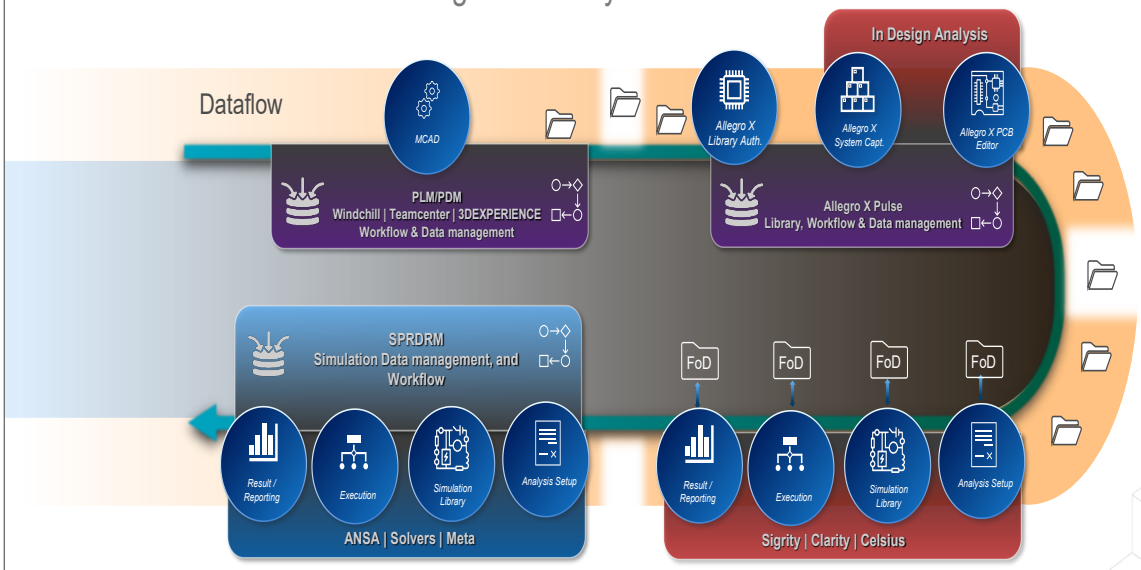
Allegro X AI On-Prem



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Opportunity For Next Level SDA Productivity

Disconnected Multidomain Design and Analysis

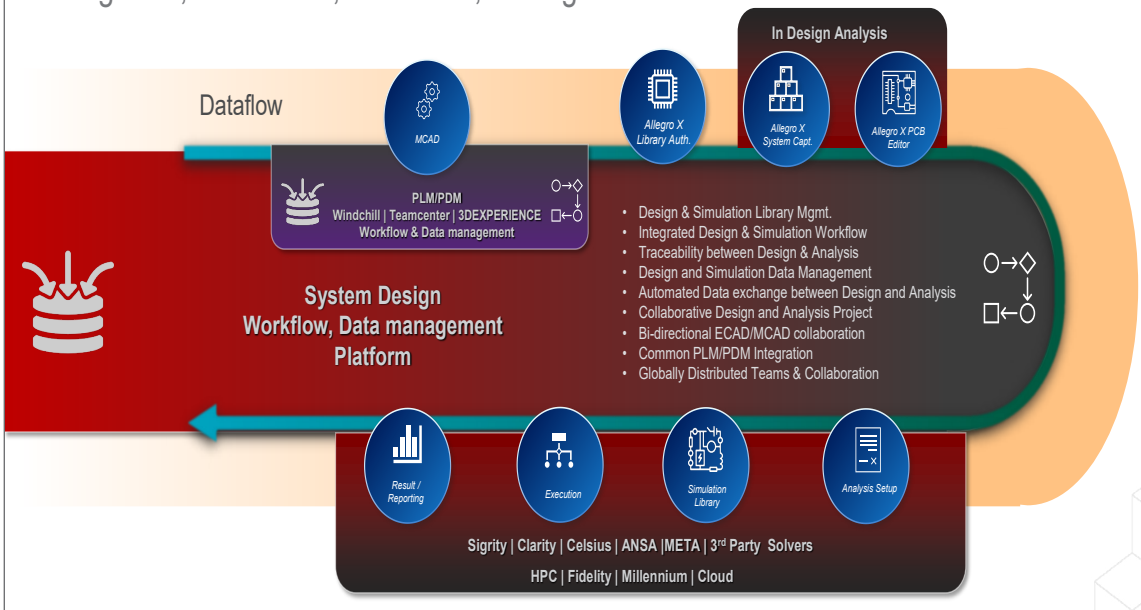


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End to End System Design and Analysis

Integrated, Automated, Traceable, Managed



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MSA Portfolio and New Technologies

Electrical, Mechanical and Digital Twin

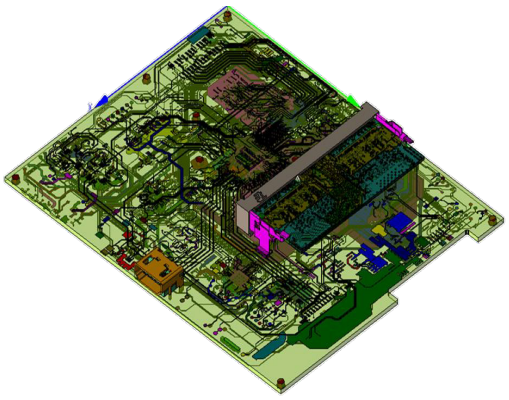
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Clarity

For 3D Electromagnetic Analysis of Electronics

- Higher performing electronics require fast and accurate 3D electromagnetic (EM) simulation as complexity increases
- Speed/accuracy of EM for in-design analysis and final system signoff
  - >10x speed up via fast and efficient distributed solver and mesh algorithms
  - Near linear scaling delivers unmatched capacity
  - Integrated workflows with schematic/layout of Allegro, APD, AWR and Virtuoso
- POR at multiple NASDAQ 100 firms delivering faster TAT on most challenging designs; >100 new logos in 2024
- What's New:
  - GPU acceleration
  - Gen AI antennas
  - Copilot
- IC, Packaging and PCB now, AI automation and GPU acceleration next…



Simulation	Legacy (Hrs)	Clarity (Hrs)	Speed Up
Interposer	12	2.25	5.3X
SiP Signal Chain	27	1.5	17.0X
Serdes Package	22.5	2.25	7.0X
HBM Wafer Level SiP	86.4	7.2	12.2X

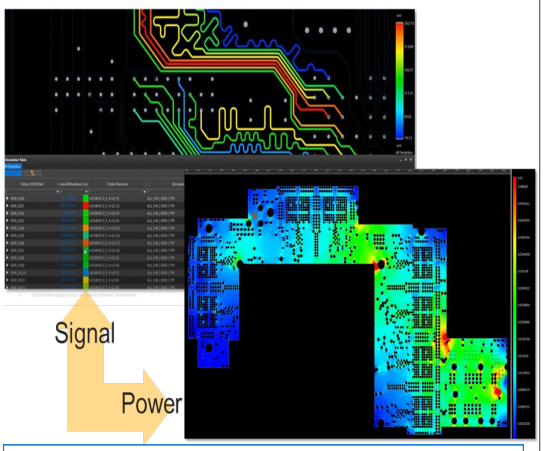
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Sigrity X

For Signal/Power Optimization and System Signoff

- PCB and IC package designers must account for end-to-end, multi-fabric, multi-board systems for signoff success
- SI/PI interconnect simulations critical to product success; leveraging in-design analysis for earlier insight decisions
  - Comprehensive signal (Transmitter to Receiver) and power (Source to Sink) analysis
  - Faster TAT and accelerated TTM
  - Improved design QoR
  - Visualization of results in Allegro, APD and OrCAD
- POR at nearly all top semi/system companies for SI/PI sign-off; >50 new logos for in-design analysis.
- What's New:
  - Faster simulation for very large PCB and Packages
  - Copilot
- IC packaging and PCB now, advanced packaging with interposer and AI automation/acceleration next…



Simulation	Legacy (#Sims)	Sigrity X (#Sims)	Speed Up
112Gb/s (CEI-112G-LR)	636,804	100	6000X
PCIe (6.0)	1278	75	17X
PCIe (5.0)	429	43	10X
DDR (LPDDR5X)	360	40	9X

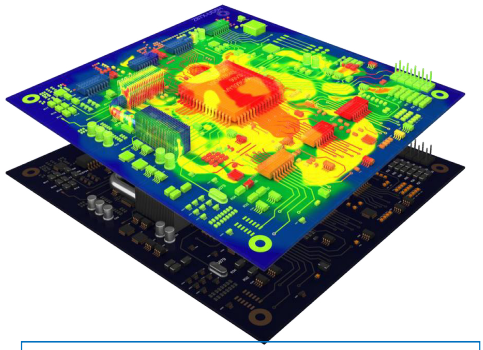
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Celsius

For Electrothermal Analysis of Electronic Systems

- Thermal issues degrade product performance and reliability
- Speed and capacity of electrothermal analysis for in-design analysis as well as final signoff
  - Full-fidelity models with no design simplifications
  - >10x faster simulation through accelerated solvers
  - Integrated workflows with schematic/layout of Allegro, APD, AWR, Virtuoso and Innovus
- POR for multiple top 10 semis and >100 new logos in 2024
  - Identifying thermal issues earlier
  - Reducing TAT 30% on average
- What's next:
  - GPU acceleration (Millennium)
  - Copilot
- IC, Packaging and PCB now, AI automation and GPU acceleration next…



Simulation	Legacy (Hrs)	Celsius (Hrs)	Speed Up
Chip/SoC	23.5	1.5	13x
Packaging	n/a	2.0	Infinite
Automotive Test PCB	n/a	2.0	Infinite
Cell Phone Enclosure	72.0	23.0	3X

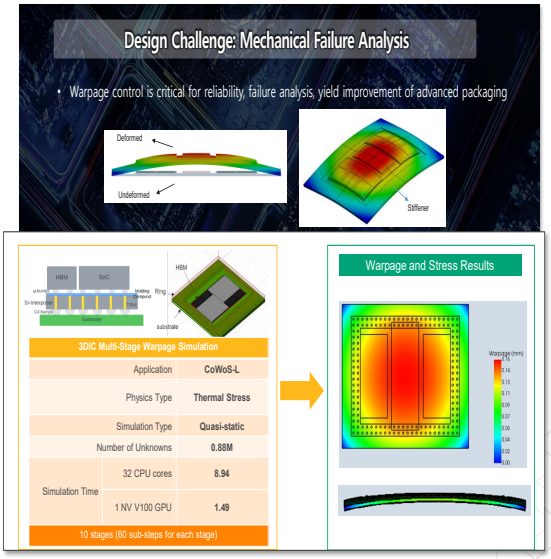
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Warpage

For electro-thermal-stress analysis for chip, package, and board

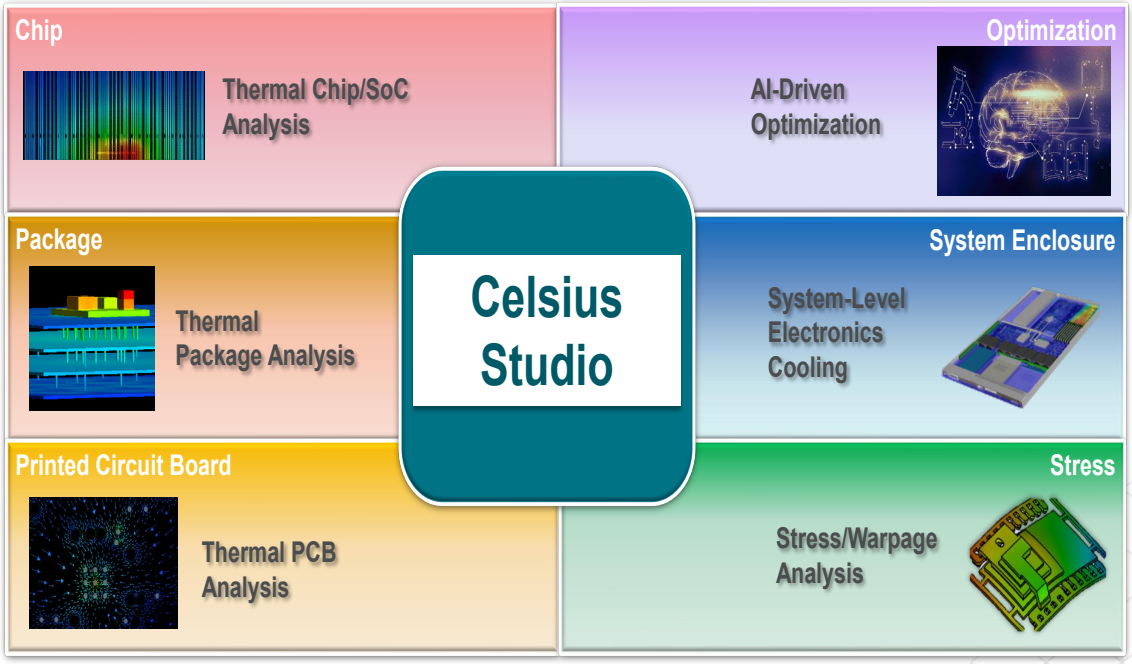
- Warpage control is a critical reliability consideration for 3DIC and advanced packaging as it can lead to mechanical failure
- Accurate simulation for early detection of silicon failure with unprecedent capacity for memory providers and ecosystem partners
  - Proven silicon accurate vs measurements within 1%
  - Uniquely addressing end-to-end warpage analysis across package assemblies and complex systems
  - Unmatched capacity with usability advantage to read native GDS vs DXF conversion
  - Streamlined workflow with Celsius Studio and Integrity
- Early access adoption by top semiconductor firms to detect warpage and improve yield on advanced process nodes
- What's New: GPU acceleration (Millennium)
- In-design stress/warpage analysis, GPU acceleration and Spectre/Virtuoso and Allegro APD workflows next…



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Thermal, Electronics Cooling and Stress/Warpage Solution



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Reality DC

For performance-aware design and lifecycle management of data centers

- Exponential growth of AI-factories requires greater efficiency of data centers' design and operation to scale to meet demand
- Optimum solution for design and operation of data center power/thermal envelope
  - Explore multiple failure scenarios
  - Minimize risk of downtime
  - Acceleration planning and deployment decisions
- POR for multiple top semi,financial and healthcare industries and >30 new logos in 2024
  - Predict potential thermal issues earlier
  - Enhance capacity planning by 2X
- What's next:
  - Liquid cooling
  - GPU solving (Millennium)
  - CoPilot
- Data centers of various size/capacity, AI modeling and regulation reporting next…



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Digital Twin Ecosystem

- 13K+ data center ecosystem "high-fidelity" models from the chip to the chiller
- Created in collaboration with data center equipment manufacturers
- Releasing AI-enabled utilities for equipment twin generation
  - Vendor creates libraries based on detailed CFD and/or performance data
  - Complex thermal behaviour simulated without tailored development
  - Seamless connection with Cadence® Celsius™ EC Solver and Cadence Reality™ DC



Celsius EC Detailed Model	Manufacturer Performance Data	Train Neural Network	Generate AI Server	Use in Data Center Digital Twin
Training simulation data generated	Additional experimental data can be supplied by manufactures	Data is used to train a neural network	An AI server is produced for use at the data center scale modelling	The library item is installed in the digital twin with AI simulating server performance

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Multiphysics Analysis CoPilots: Driving Automation and Intelligence

Bridging the gap between data center designers, operators & electrical/mechanical engineers

Cadence® Reality™ DC Copilot

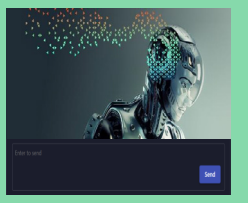
Performance

- Identifies cooling issues
- Offers recommendations
- Applies fixes, re-solves, and reports



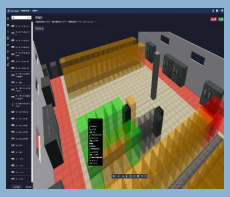
Assistant

- Q&A documentation
- Drive tools and functions
- Rule development for expert systems



Capacity

- Cabinet/server deployment recommendation
- Optimisation of energy
- Connection to Optimality™ Explorer



Calibration

- Calibration health check
- Auto-calibration guidance via optimization techniques



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Millennium 2000

Supercomputing Platform for Multiphysics CFD Analysis

- Modern scalable HPC architecture preloaded with Cadence Solvers
  - Cloud and on-prem
  - Multiple boxes can be connected
- Solver codes refactored for GPU optimization
  - GPU Computing unlocks “100X Thinking”
- What’s next: Expansion of multiphysics solvers
  - Fidelity
  - Voltus, Celsius, Warpage
  - Clarity



Simulation	1000 CPU runtime (hrs)	Millennium runtime (hrs)	Speed Up
Automobile Drag	195	6	32.5X
Turbofan Acoustics	57	2	28.5X
Aviation Combustor Heat Transfer	75	2.5	30.0X
Airframe Stall	98	3	32.7X

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GPU Acceleration Platform for Multiphysics

Supercomputing Platform for Multiphysics Analyses

- Unprecedented performance
  - 1 Millennium (32 GPUs) = 10000 CPU cores
  - Optimized with the latest GPU (A100/H100/L40S)
- Multiphysics solvers (Power/EM/Thermal/Stress)
- Scalable and flexible: Cloud & On-premise
  - Multiple Millennium boxes can be connected
- AI data generation, training and inference on a single Millennium



Simulation	512 CPU runtime (hours)	Millennium runtime (hours)	Speed up
Voltus	120	6	20X
Clarity	48	6	8X
Celsius	39	2.5	16X
Warpage	20	2	10X

20X Power Savings @ iso-performance

Co-optimized with NVIDIA Accelerated Compute & AI Platform

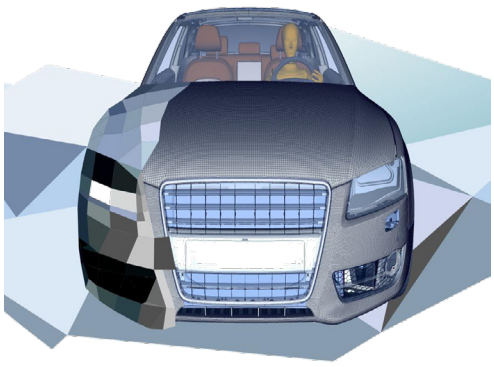
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Beta CAE ANSA

For In-Design Analysis of Physical Systems

- Physical systems are everywhere and growing in complexity, inclusive of size, scope, components, and teams
- An integrated workflow is essential to design, analysis and optimization of components through to complete subsystems and systems
  - Modern cockpit for engineering productivity and faster TAT
  - In-design analysis of structural, mechanical and CFD multiphysics
- POR for all automotive OEMs and their suppliers; global high-tech and aerospace industry leaders
- What's New:
  - Multiphysics expansion to CFD
  - Multiphysics expansion to EM and Thermal
  - AI-enabled optimization, training and inference
- Automotive and A&D crash and aerodynamics analyses now, system-level EM and thermal next …



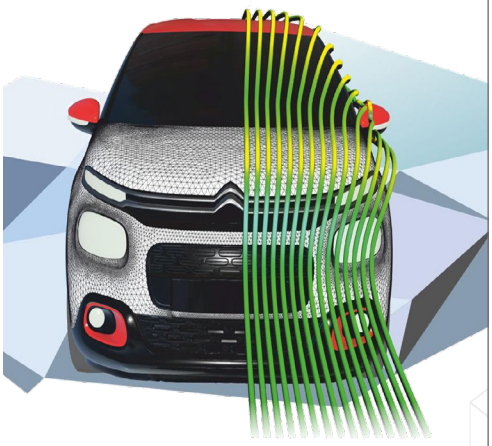
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Beta CAE META

For Visualization and Optimization of Physical Systems

- Physical systems are everywhere and growing in complexity, inclusive of size, scope, components, and teams
- An intelligent, integrated workflow is essential to design, analysis and optimization of components to subsystems and complete systems
  - Multi-disciplinary insights via integrated post-processing and data analysis
  - Advanced visualization of results featuring high performance graphics and virtual reality
  - Full automation of process steps including report generation
- POR for all automotive OEMs and their suppliers; global high-tech and aerospace industry leaders
- What's New:
  - Enhanced visualization
  - Post-processing integrations
  - AI-driven insights
- Automotive and A&D Physical systems, electronic systems next …

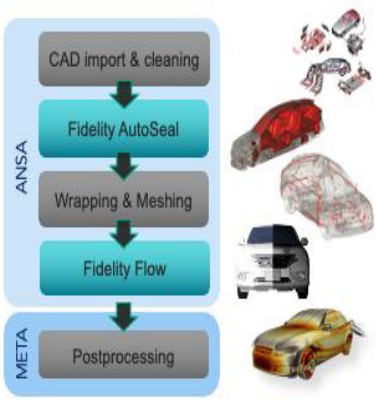


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Beta CAE In-Design with Fidelity CFD

For In-Design Physical Fluid Dynamics Analyses

- Right the first-time design of Physical systems requires fast and accurate computational fluid dynamics (CFD) simulations
- Fidelity provides predictive in-design CFD with high-fidelity results quickly for automotive and A&D markets
  - >10X speed-up via scalable, GPU-resident solver technology
  - Large eddy simulator (LES) for full system sign-off in hours for design decisions within the day
  - Streamlined workflows combining Fidelity with Beta CAE and AI-enabled optimization accelerates TAT by >20x
- POR at automotive OEMs (tier 1 & 2) as well as A&D delivering faster TAT workflow vs legacy point tools
- What's next:
  - GPU-acceleration (RANS)
  - Fidelity + Optimality
  - AI prediction (Celerity)
- Automotive, A&D, turbo and marine CFD analyses today, GPU acceleration and workflow automation next…



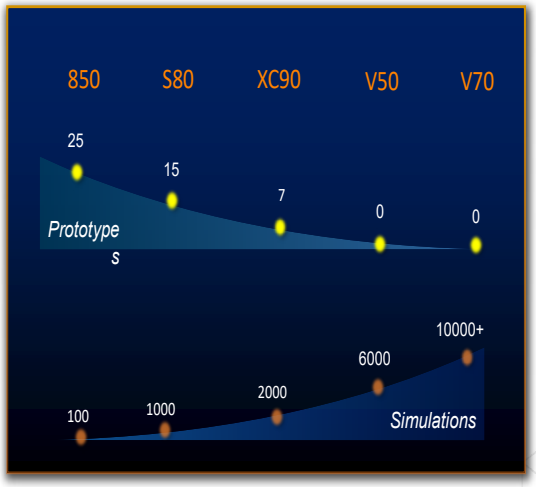
OEM	Legacy Workflow TAT	Beta CAE + Fidelity IDA Workflow TAT	Speedup
Car maker 1	15 days	5 h	70X
Car maker 2	7 days	6 h	30X
Car maker 3	20 days	7 h	70X
Car maker 4	30 days	9 h	80X

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Beta CAE In-Design with Epilysis Mechanical

For Structural Analysis of Electronic and Physical Systems

- Mechanical/structural analysis of automotive and A&D systems are growing exponentially to meet safety requirements
- Linear and non-linear structural analyses critical to end-product success and right-the-first-time design
  - Virtual prototyping reduces reliance on physical test
  - Accurate in-design analyses for structural multiphysics
  - >5x productivity boost through in-design analysis workflow
  - Streamlined design cycle accelerates TAT
- Structural/mechanical in-design analysis at 2000+ Physical system firms including automotive OEMs, suppliers, high-tech and aerospace accounts
- What's next:
  - AI-optimization
  - Explicit dynamics solver for drop testing
- Automotive and A&D FEA and NVH now, impact FEA and drop testing next …



Prototypes v Simulations Trend for Volvo Models YoY

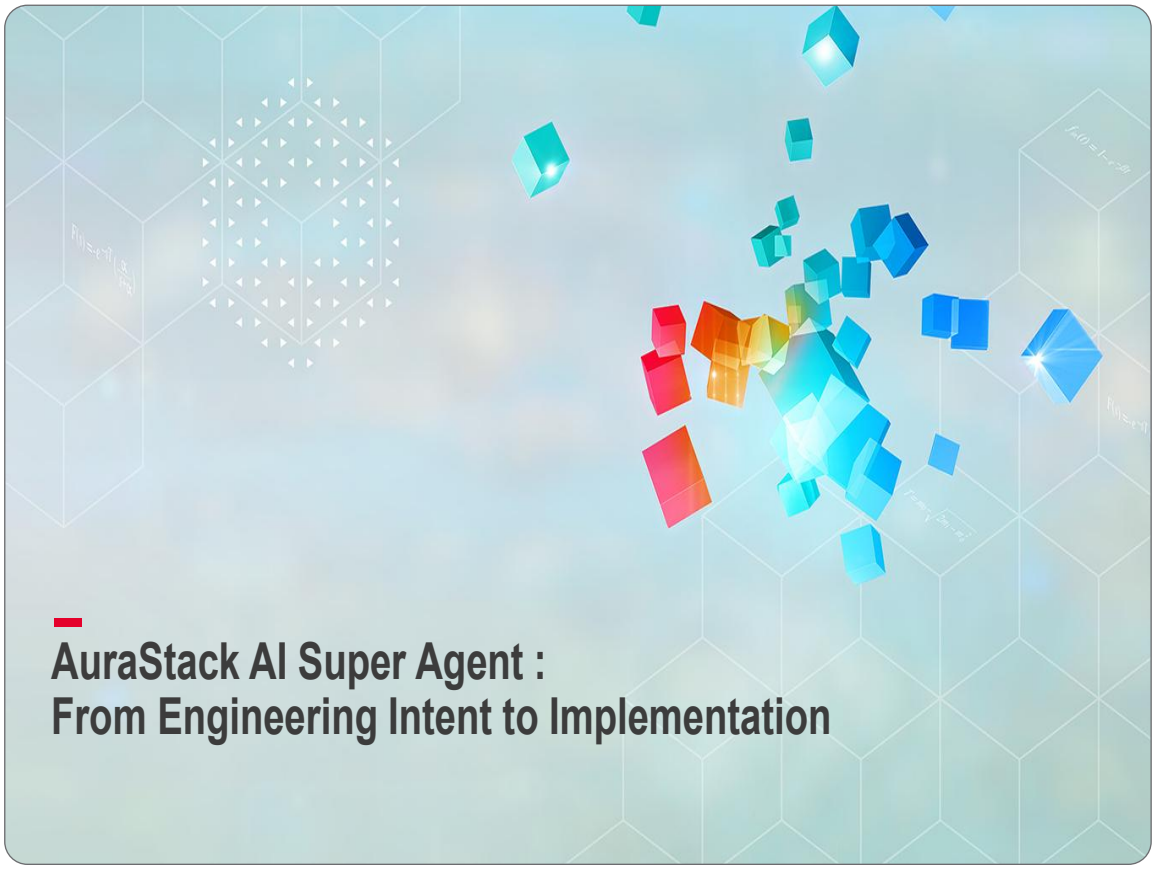
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AuraStack AI Super Agent : From Engineering Intent to Implementation

오 영 주
(Cadence Korea)


AuraStack AI Super Agent :
From Engineering Intent to Implementation

Memo

Clarity / Sigrity Technologies : What's New & Roadmap

김 성 주
(Cadence Korea)



Memo

PLM 기반 OrCAD Capture CIS Interface 구축 사례

이 수 열
(HL Klemove)



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HL Klemove 소개

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05 **Effect & Lessons**
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01 COMPANY

HL Klemove Snapshot

자율주행 · ADAS 전문 기업, 글로벌 엔지니어링 · 생산 거점 운영

1.8조	20.4%	2,900+	AD / ADAS
'25 매출	'26~'30 CAGR	임직원	Automotive Electronics



Global Footprint

8	Engineering 4 Tech Centers 포함	4	Plants KR · CN · MX · IN
9	Sales Offices	4	Vehicle Test

Global Market Share ('25)

Front Camera	5위	7.5%	누적 출하 2,390만
Front Radar	4위	6.2%	누적 출하 1,770만

※ 누적 출하 '10~'25, HKL internal analysis

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01 COMPANY

Product & Manufacturing

레이더 · 카메라 · HPC부터 전장 ECU까지, 모든 제품의 중심에는 PCB가 있습니다



자율주행 솔루션

- 레이더 : 전방 · 코너 · 4D 이미징
- 카메라 : Smart · Satellite · DMS / OMS
- HPC : 주행 · 주차 · 통합 제어기, ZCU



전장 솔루션

- 제동 · 조향 ECU, 2W ABS ECU
- AVAS · TAS · SCR · FPC · WSS
- EMS : 전장품 Built-to-Print 생산



로봇 & 모빌리티

- Robot Sensor : 환경 인식 · 위치 / 모션
- Mobility Sensor

Global Manufacturing 4개 공장 · 총 100개 라인

SMT	Radar	Camera	HPC	Chassis ECU	AE
26 lines	10 lines	5 lines	3 lines	37 lines	19 lines
연 4,285만 pcs	SRR · MRR · LRR	FCM	APCU · ADCU · HPC	제동 · 조향 · 현가	TAS · WSS · AVAS

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02

Background

회로 설계 환경 변화와 문제점

설계 환경의 변화 · 현상 및 문제점

데이터로 본 Library 현황

왜 BOM 자동화인가

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02 BACKGROUND

설계 환경의 변화

제품 · 부품 · 설계 인력은 늘었지만, Library와 BOM 관리 방식은 그대로

제품 · 모델

다변화

레이더 · 카메라 · HPC 등
제품군과 파생 모델 증가

제품별 설계 기준 · 부품 표준 다양화

전자부품

약 1만 건

PLM에 등록된 전자부품

매년 약 500건 신규 등록

협업 범위

확대

회로 → PCB → 생산 → 협력사로
이어지는 협업

설계 인력 · 사이트 간 협업 증가

그런데, 회로 Library와 BOM은 여전히 '개인'과 '엑셀'에 의존

설계 규모는 커졌지만 Library · BOM · 도면 관리는 개인 PC와 수작업 중심으로 남아 있었습니다

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02 BACKGROUND

현상 및 문제점

Library · 프로세스 · 시스템, 세 곳의 '단절'이 설계 품질과 생산성을 떨어뜨림

LIBRARY

개인별 Library 관리

- 담당자별로 각자 Library 작성
- 약 1만 건을 엑셀로 분산 관리
- 중복 작성, 속성 구조 제각각

영향 **중복 · 불일치**

PROCESS

등록 · 검증 프로세스 부재

- 등록 · 검토 · 승인 절차 없음
- Schematic ↔ PCB 연동 부족
- 좌표 오류를 생산 단계에서 발견

영향 **생산 단계 오류**

SYSTEM

PLM 연계 단절

- 도면 PDF 변환 후 수동 업로드
- 엑셀로 BOM 수작업 구성
- 원본 · 이력 추적 어려움

영향 **수작업 · 이력 단절**

개인별 Library → 비표준 데이터 → 수작업 BOM → 생산 단계 오류

정합성을 '사람'이 맞추는 구조, 개선이 시급했습니다

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02 BACKGROUND

데이터로 본 Library 현황

PLM 전자부품 약 1만 건 분석으로 정비 대상과 우선순위를 도출

약 1만 건

PLM 등록 전자부품

개인별 Library로 분산 관리

64%

RLC 비중

저항 · 콘덴서 · 인덕터 일괄 정비 효과 큼

약 300건

데이터 이슈

중복 Ordering No Maker No · Spec 누락

약 40%

최근 3년 실사용 부품

실제 BOM에 쓰인 부품 우선 구축 대상

부품 구성

RLC (저항 · 콘덴서 · 인덕터) 64% | IC · Diode · FET · MCU 등 36%

전사 통합 관리
개인별 관리 → 전사 단일 Library

표준화 · 공용화
유사 · 중복 부품 정리, 재고 감소

우선순위 구축
실사용 부품부터 단계적 정비

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02 BACKGROUND

왜 BOM 자동화인가

설계는 끝났는데, BOM은 다시 사람이 만들었습니다

회로와 PCB 설계를 마치면 Partlist를 엑셀로 뽑고, 좌표를 붙이고, BOM을 다시 손으로 구성해 PLM에 올렸습니다.

이 과정에서 생긴 작은 실수는 생산 단계에서야 드러났고, 설계가 바뀔 때마다 같은 작업을 되풀이해야 했습니다.

그동안

엑셀로 옮겨 만드는 BOM

품번 오기 · 누락, Top / Bottom 구분 오류
설계 변경 때마다 반복되는 수작업

이제는

설계 결과가 그대로 BOM으로

Check-in 한 번으로 BOM 생성부터 PLM 등록까지
사람 손을 거치지 않아 오류가 없고, 설계자는 설계에 집중

핵심 설계 결과를 BOM으로 자동 변환하여 휴먼 에러를 없애고 작업 시간을 줄이는 것

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03

Solution

CIS Library 통합 · 설계 표준화 · PLM Interface

해결 방향 · 시스템 구성

Library 통합 · 등록 프로세스

PLM-OrCAD Interface · BOM 자동화

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03 SOLUTION

해결 방향 : 3대 추진 전략

Library 통합 → 설계 표준화 → PLM Interface, 설계에서 BOM까지 하나의 흐름으로

01 CIS Library 통합

- 통합 CIS Library DB 구축
- 부품 속성 · 명명 표준화
- PLM EPDB 부품 정보와 연계

개인 Library → **전사 단일 Library**

02 설계 업무 표준화

- Library 등록 · 승인 프로세스
- Symbol · Footprint 표준 체계
- Library 담당자 R&R 정립

사람 의존 → **프로세스 기반**

03 PLM Interface

- OrCAD에서 바로 Check-in / out
- BOM 자동 구성 (Top / Bottom)
- 도면 · 파일 · 이력 자동 관리

수작업 업로드 → **자동 연계**

원칙 1 부품 정보의 기준은 PLM

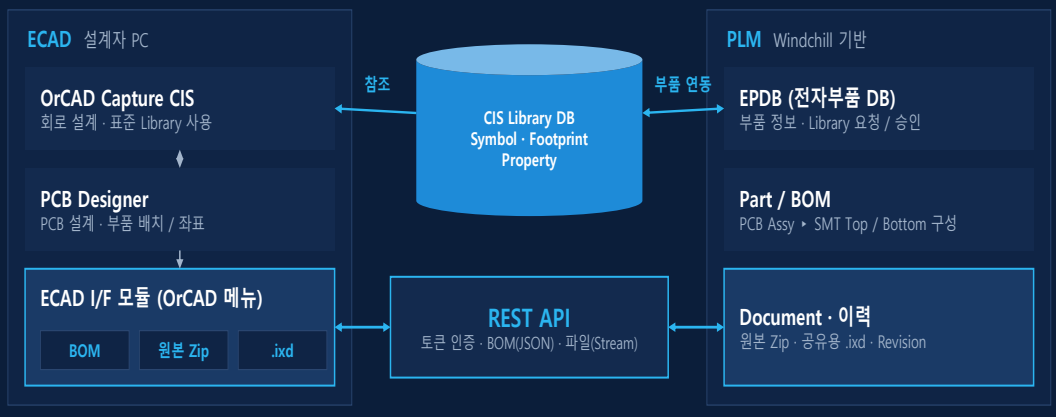
원칙 2 ECAD 버전에 영향 없는 표준 Interface

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03 SOLUTION

PLM-ECAD Interface 구성도

부품 정보는 PLM(EPDB)에서, 설계 결과(BOM · 도면 · 이력)는 다시 PLM으로



유관부서 · 협력사
.ixd Viewer로 ECAD 없이 도면 열람

생산 · SMT
PLM BOM · 좌표(X · Y · Angle) 활용

기구 설계
기구 · 회로 데이터를 PLM에서 통합 협업

※ ECAD I/F : Interxsoft 협업 구축

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03 SOLUTION

CIS Library 통합 · 구축 전략

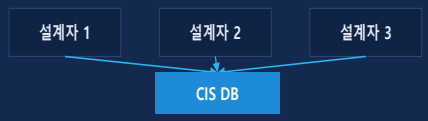
사용자별 Local Library에서 통합 CIS Library로, 실제 사용 부품부터 단계적 구축

AS-IS OrCAD Capture (사용자별 Local Library)



저장 위치	사용자별 Local 폴더
관리 방식	사용자별 개별 관리
부품 정보	사용자마다 분산 · 상이

TO-BE OrCAD Capture CIS (통합 CIS Library)



저장 위치	**네트워크 통합 Library DB**
관리 방식	**Library 담당자 일괄 관리**
부품 정보	**PLM EPDB 기준 공통 참조**

구축 · 운영 전략

우선순위 구축
- 최근 3년 실제 BOM 사용 부품부터
- RLC는 표준화 전제로 일괄 정비

단계적 전환
- 신규 설계는 CIS 기반 작성 원칙
- 기존 도면은 신규 설계 시점에 전환

운영 체계 (R&R)
- Library 담당자 · 표준화 협의체
- I/F 필수 Property 가이드 제공

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03 SOLUTION

Library 등록 · 승인 프로세스

PLM에서 요청하고, 담당자가 작성하고, 설계자가 검토한 Library만 배포

자재관리	설계자	설계자	Library 담당자	설계자	Library 담당자
STEP 1	STEP 2	STEP 3	STEP 4	STEP 5	STEP 6
품번 생성	**Library 조회**	**등록 요청**	**작성 · 등록**	**검토**	**승인 · 배포**
품번 등록 · 승인	EPDB 부품 검색	요청서 작성	CIS DB 등록	Library 확인	RELEASED

→ → → → →

Reject 시 재작성

Library Status 관리

NONE	INWORK	INWORK	RELEASED	RELEASED
INACTIVE	INACTIVE	INACTIVE	ACTIVE	INACTIVE
Library 없음	요청 접수 · 작성 중	설계자 검토 중	**배포 · 설계 사용**	수정 · 사용 중지

※ Library 요청서 : 요청 유형(New / Change) · 기한 · Symbol / Footprint / Datasheet 첨부 · 담당자 메일 알림 · 이력 관리

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03 SOLUTION

PLM-OrCAD Interface 업무 시나리오

OrCAD에서 Check-in 한 번으로 BOM · 원본 도면 · 공유용 파일을 PLM에 자동 등록

ECAD 설계자 PC

1 회로 설계	2 PCB 설계	3 I/F 메뉴 실행	4 관리정보 입력	5 Check-in
OrCAD Capture CIS 승인 Library 사용	PCB Designer 배치 · 좌표	OrCAD 메뉴에서 PLM 토큰 로그인	PCB Assy 품번 SMT Top / Bottom	Auto Run(Batch) BOM · Zip · .ixd 생성

REST API 전송 BOM : JSON | 원본 Zip · .ixd : Stream | 사전 Validation : PLM 품번 존재 · BOM 구성 Rule

PLM Windchill 기반

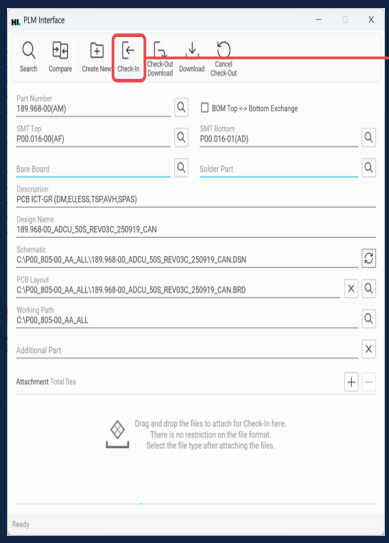
6 BOM 자동 구성	7 도면 · 파일 첨부	8 Revision 관리	9 조회 · 활용
PCB Assy 하위 SMT Top / Bottom BOM	원본 Zip + .ixd를 Part에 자동 첨부	Check-in / out · Undo 버전 이력 자동 기록	PLM에서 BOM 확인 ECAD 없이 도면 열람

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03 SOLUTION

Interface 주요 기능 · 화면

설계 툴을 벗어나지 않고, 한 화면에서 검색부터 Check-in · Download까지



Search	PLM 등록 도면 조회, Working 도면과 비교
Compare	현재 열린 도면과 PLM 도면 비교
Create New	도면 최초 등록, SMT Top / Bottom 지정
Check-in	도면 + BOM PLM 등록, Revision 자동 증가
Check-out	PLM 상태 변경 (편집 잠금)
Download	원본 Zip · 공유용 .ixd 다운로드
Cancel Check-out	Check-out 취소, 상태 원복

Check-in 사전 Validation

BOM 부품의 PLM 품번 등록 여부와 BOM 구성 Rule을 먼저 확인
잘못된 데이터가 PLM에 들어오지 않도록 차단

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03 SOLUTION

BOM 작성 · 등록 자동화

엑셀 Join과 수작업 BOM 구성을 없애 BOM 등록 4단계 → 2단계

AS-IS 4단계 (엑셀 수작업 2회)

1. 회로 / PCB BOM 엑셀 Join 수작업
2. PLM 채번 (PCB Assy · SMT Top / Bottom)
3. 엑셀로 BOM 구성 · 확인 수작업
4. PLM 수동 Upload + 도면 PDF 첨부

TO-BE 2단계 (엑셀 수작업 0회)

1. PLM 채번 (PCB Assy · SMT Top / Bottom)
2. Check-in 화면에서 품번 선택 → 자동 등록

시스템이 자동 처리
Partlist + PCB 좌표 자동 결합 (Ref. Des · X / Y · Angle)
SMT Top / Bottom 구분, 원본 Zip · .ixd 생성 및 첨부

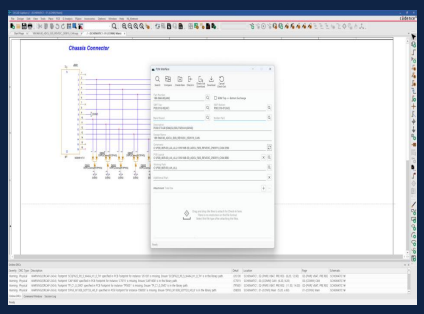
4 → 2	0회	자동
BOM 등록 단계	엑셀 수작업	SMT Top / Bottom 구분

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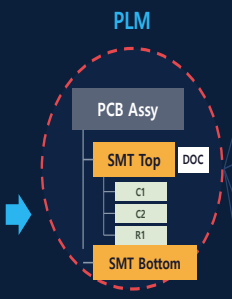
03 SOLUTION

설계 데이터 통합 관리 · 공유

원본 도면 · 공유용 파일 · BOM · 이력을 PLM 한 곳에서, ECAD 없이도 열람



OrCAD에서 Interface 실행



BOM 자동 구성 · 파일 첨부
PCB Assy ▸ SMT Top / Bottom

원본 도면
dsn · brd · opj 원본을 Zip으로 첨부

공유용 파일 (.ixd)
ECAD 없이 Viewer로 열람 · 공유

BOM · 좌표
Top / Bottom BOM, 좌표를 생산과 공유

Revision 이력
Check-in / out으로 이력 자동 기록

기구 CAD(CATIA) · 회로 CAD(OrCAD)를 하나의 PLM에서 통합 관리

▶ 데모 영상

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04

Validation

현업 PoC로 먼저 검증하고, 단계적으로 구축

추진 경과

현업 PoC 평가 결과

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04 VALIDATION

추진 경과

PoC로 방향을 검증한 뒤 Interface 개발과 Library 통합을 병행

'25.12	'26.01	'26.03	'26.03 ~	'26.07	'26.09 ~
현업 PoC	**수행계획**	**분석 · 설계**	**개발 · 테스트**	**Library 착수**	**확대 · 적용**
엔지니어 대상 연동 데모 · 평가	범위 · R&R 확정	I/F Rule 정의 화면 설계	BOM · 첨부 모듈 단위 · 통합 테스트	H/W 대상 CIS 데모 전사 Library 구축	우선 대상 구축 제품별 적용 확대

Interface 개발 계획 (약 10주)

계획 1주	분석 · 설계 1주	시스템 개발 : ECAD I/F · PLM API 6주	테스트 · 이행 2주

착수 · 팀 구성 → 인터뷰 · I/F Rule 정의 · TO-BE 설계 · 로그인(SSO) 방식 정의 → 개발 → 단위 · 통합 테스트 → 이행 · 안정화

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04 VALIDATION

현업 PoC 평가 결과

회로 · PCB 엔지니어 평가 98.9% PASS : 현업 프로세스와 일치, 개선 효과 기대

PASS Rate

98.9%

PASS 178건 / 180건

평가 영역

- 업무 프로세스 일치성
- BOM 연계 (Partlist · 좌표)
- 설계 도면 연계 · Viewer
- 도입 효과 · 운영성

영역별 PASS 비율



주요 현업 의견

긍정	회로 CAD에서 도면 · BOM까지 생성되는 흐름 확인
긍정	BOM 수작업 공수 감소 BOM Import 시간 단축 기대
긍정	interCAD Viewer 사용성 양호
요청	I/F 필수 Property 가이드 제공
요청	Top / Bottom 생산 협의 확인 Viewer 설치 편의성 개선

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05

Effect & Lessons

기대효과 · Lessons Learned

기대효과

Lessons Learned

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05 EFFECT & LESSONS

기대 효과

설계에서 BOM까지 끊김 없이 연결해 품질 · 생산성 · 협업을 함께 개선

		개선 전	개선 후
품질	표준 Library 기반 설계	개인별 중복 · 비표준 Library	→ 승인된 전사 통합 Library만 사용
생산성	BOM 자동 구성	엑셀 Join · 수작업 BOM (4단계)	→ Check-in 시 자동 구성 (2단계)
양산 품질	오류 사전 차단	Partlist · SMT 좌표 오류를 생산에서 발견	→ 설계 단계 자동 생성 · 사전 Validation
협업	설계 데이터 단일 관리	PDF 수동 업로드 · 개인 보관	→ 원본 · 공유용 · BOM · 이력 PLM 통합

Next 표준화된 부품 · BOM 데이터를 기반으로 AI를 활용한 BOM · 부품 데이터 정합성 검증

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05 EFFECT & LESSONS

Lessons Learned

Interface는 수단, 성패는 Library와 운영 체계가 결정합니다

01	Interface보다 Library가 먼저	I/F 개발은 수 주, Library 정비는 장기 과제
02	부품 정보의 기준은 PLM	EPDB 기준으로 CIS Library와 연동해 불일치 차단
03	데이터는 사전에 검증	Check-in 시 품번 · BOM Rule을 먼저 확인
04	Tool 독립적 표준 Interface	CAD 버전과 무관한 REST API 구조
05	사람과 R&R이 지속성을 결정	담당자 · 협의체 · 등록 프로세스가 운영을 좌우

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감사합니다

Q & A

이수열 책임매니저 | HL Klemove IT팀

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Integrity System Planner를 활용한 Package Connectivity Check & Verification

김 수 정
(HANA Micron)


Integrity System Planner를 활용한
Package Connectivity Check & Verification

Memo

Next-Generation 3D-IC Design and Verification Platform

박 용 진
(Verity Technology Korea)



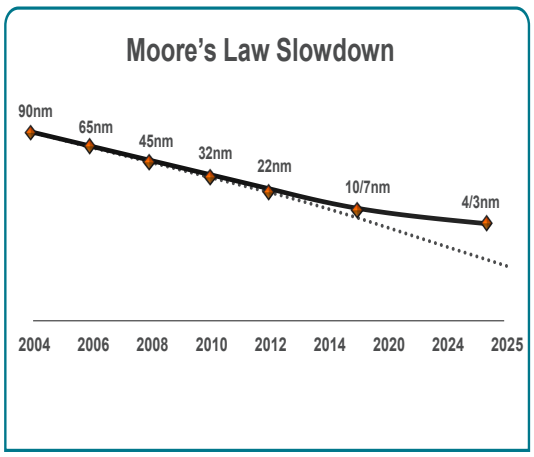
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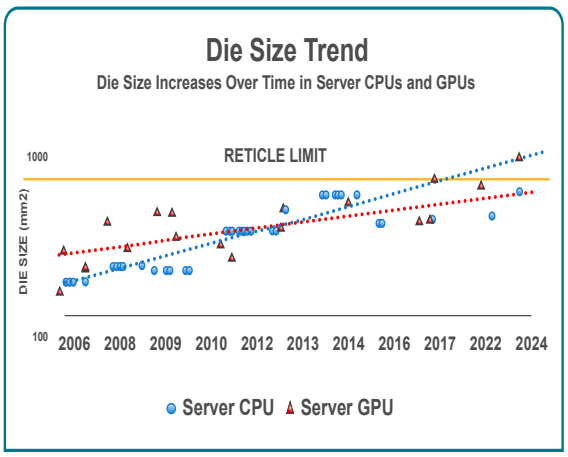
- Overview & 3D-IC 배경 및 과제
- Cadence Integrity 3D-IC Platform 소개
- 3D-IC System Planning and Co-Design
- Early Analysis 및 Verification / Signoff 솔루션
- Q & A

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Moore's Law Slowing and Die Size Reaching Lithography's Reticle Limit





Advanced Nodes Reaching Physical Transistor Size Limit

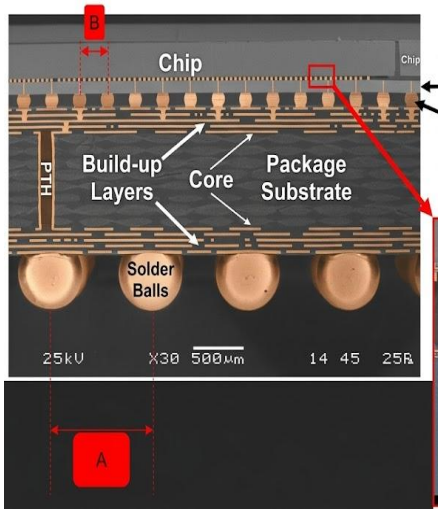
Die Sizes Increasing at an Unsustainable Rate

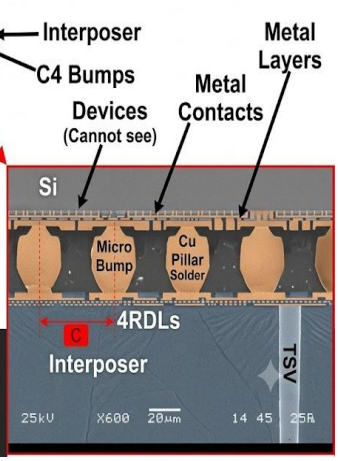
Source: Delivering the Future of High-Performance Computing, AMD keynote, Dr. Lisa Su, Hotchips, August 2019

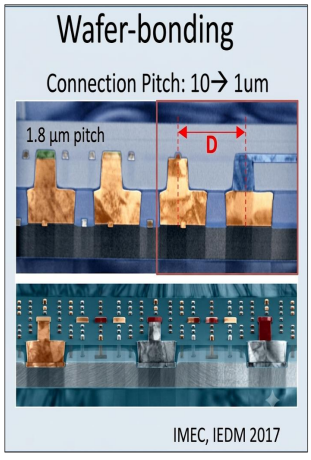
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Chip-to-Chip Connection Roadmap – Wafer Level







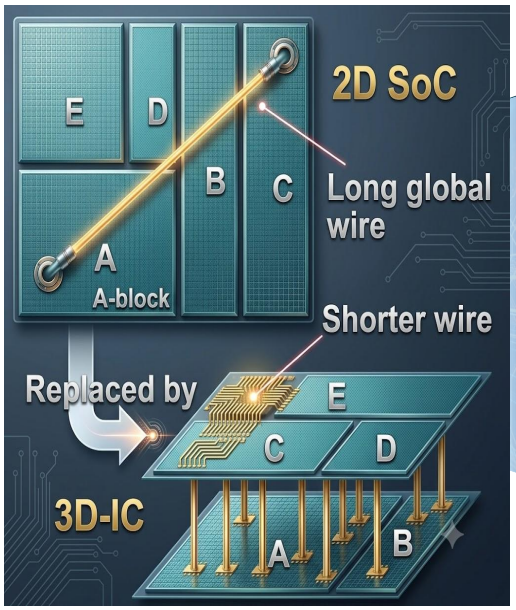
Connection Type	Solder Ball	C4 Bump	Micro Bump	Hybrid Bond
Typical Pitch of Connection	A >1000um	B 250um	C 50um	D <10um
# of Connection (in 1mm² area)	<1	16	400	>10000

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資料来源：Semiconductor Advanced Packaging，John H. Lau

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What 3D-IC can offer





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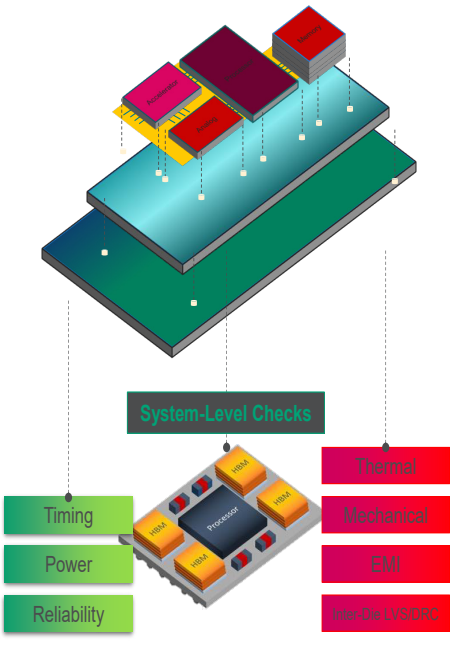
3D-IC Design Challenges

- 3D-IC design aggregation and management
  - Die placement and bump planning
  - SoC and packaging teams works in silos
  - No single database to represent multiple technologies
- Additional system-level verification
  - Thermal analysis from across chip(lets) and package
  - 3D STA with explosion of corners for signoff
  - Inter-die connectivity validation at the system level

☒ Current industry solutions: **Disjointed, point solution-based**

☒ No way to do exploration / **early feedback**

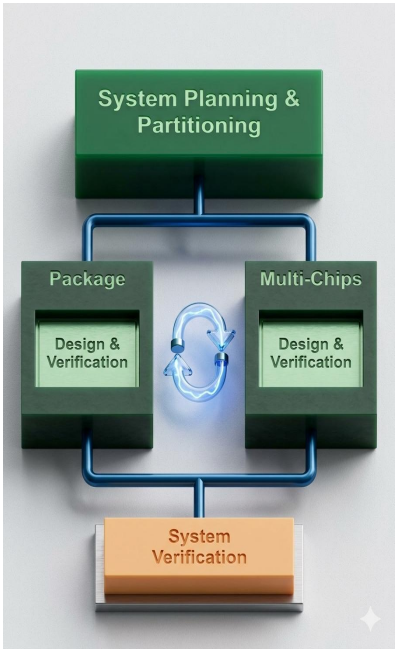
☒ **Causes costly overdesign of individual dies in a stack**



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Ideal Solution : Full 3D-IC Design Flow



- System Partitioning, Planning
- Implementation with System driven PPA
- Thermal and Power (Early Analysis and Signoff)
- Integration (Analog and Package co-design)
- Multi-Die Timing Signoff
- Multi-Die Physical Verification
- Testing for 3D & 2.5D Die Stacks (IEEE 1838)

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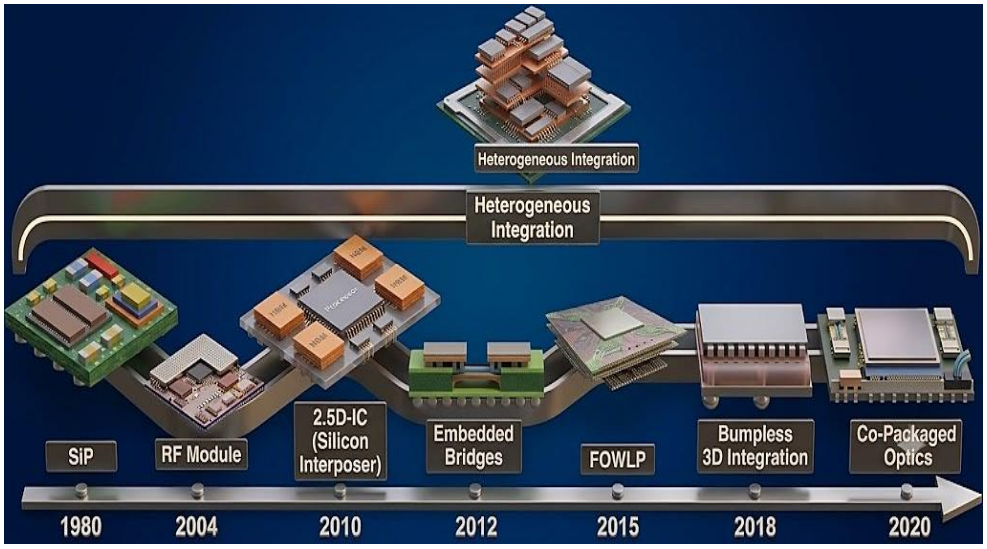
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Cadence 3D-IC Platform Solution

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본 자료는 VTK의 자산이며 무단 복제·배포·재 배포(2차 공유)를 금합니다. Cadence 및 관련 로고/상표는 Cadence Design Systems, Inc.의 소유입니다.

cadence CHANNEL PARTNER

Cadence Advanced Multi-Chip(let) Packaging Leader



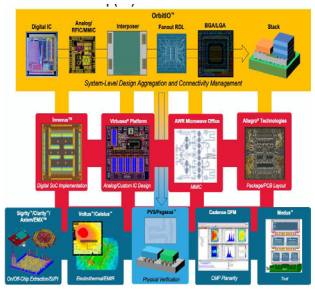
Over 20+ years of customer success driven by digital, analog & package design

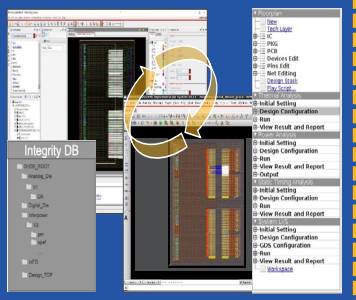
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Cadence Integrity 3D-IC Platform Evolution

Cadence® Integrity™ 3D-IC Platform







2019

- Complete 2D and 2.5D-/3D-IC packaging flows
- Stand-alone tools
- Complex work-flows

Point-Tool Centric

2020-2021

- Integrated multi-die planning and implementation
- Allegro co-design
- 3D-IC signoff & system analysis flows
- Integrity database

Direct Integration

Q4 2021 ~

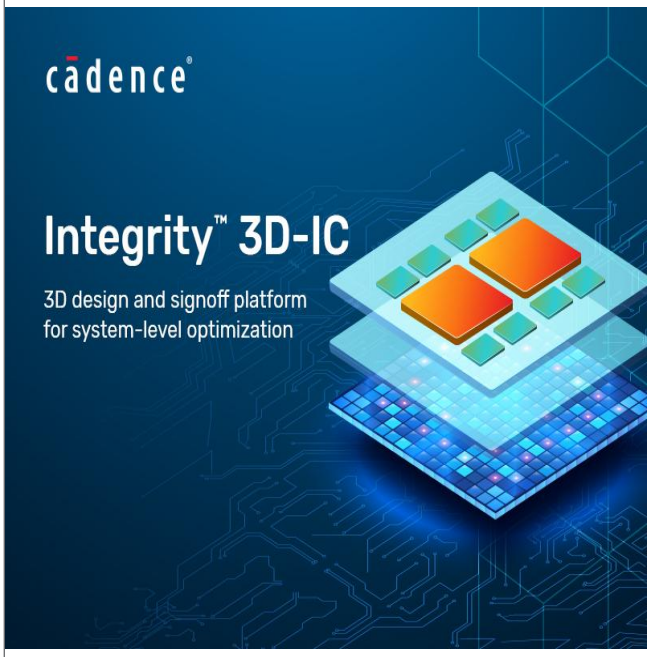
- Cross-die optimization
- System-driven PPA considering thermal and power
- Virtuoso co-design
- Advanced multi-chip(let) STA

Platform

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Introducing Integrity 3D-IC



Integrated 3D design planning and implementation

Early 3D thermal, power, and static timing analysis (STA)

Comprehensive system enabling system-driven PPA

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Recent 3D-IC Announcements

Cadence Accelerates System Innovation with Breakthrough Integrity 3D-IC Platform

Industry's first comprehensive 3D-IC platform for multi-chiplet design and advanced packaging

SAN JOSE, Calif., 06 Oct 2021

Highlights:

- *Integrity 3D-IC integrates design planning, implementation and system analysis in a single, unified cockpit*
- *Designers can achieve system-driven PPA through the availability of integrated thermal, power and static timing analysis capabilities*
- *Cadence's third-generation 3D-IC solution supports a wide range of application areas, including hyperscale computing, consumer, 5G communications, mobile and automotive*

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Cadence Integrity 3D-IC Platform Supports TSMC 3DFabric™ Technologies for Advanced Multi-Chiplet Designs

SAN JOSE, Calif., 26 Oct 2021

Highlights:

- *The Cadence 3D-IC solution centers on the Integrity 3D-IC platform, which provides integrated planning, implementation and system analysis to optimize PPA for multi-chiplet systems*
- *The Tempus Timing Signoff Solution with inter-die analysis and STA technologies results in faster time to tapeout*
- *The Voltus IC Power Integrity Solution, tightly coupled with the Celsius Thermal Solver, facilitates multi-die IR drop and thermal analysis for design robustness*
- *Customers can confidently adopt the Cadence 3D-IC solution and TSMC 3DFabric technologies to create next-generation hyperscale computing, mobile and automotive applications*

Cadence Integrity 3D-IC Platform Qualified by Samsung Foundry for Native 3D Partitioning Flow on 5LPE Design Stack

SAN JOSE, Calif., 17 Nov 2021

Highlights:

- *Integrity 3D-IC is Cadence's next-generation multi-chip design solution, integrating silicon and package planning and implementation with system analysis and signoff to enable system-driven PPA optimization*
- ***Native 3D partitioning flow** automates intelligent creation of memory-on-logic 3D stacking configuration, providing PPA improvements for 3D stack designs*
- *Customers can confidently adopt the Cadence Integrity 3D-IC platform and Samsung Foundry's multi-die implementation flow to create next-generation hyperscale computing, mobile, automotive and AI applications*

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Integrity 3D-IC Customer Experience

"With 3D-IC design continuing to gain momentum, there is an increased need to automate the planning and partitioning of a 3D stack die system more efficiently. As the world-leading research and innovation hub in nanoelectronics and digital technologies and through our longstanding collaboration with Cadence, we've successfully found automated ways to partition designs to build an optimal 3D stack with increased accessible memory bandwidth that pushes performance and lowers power in advanced-node designs. The integrated memory on the logic flow included in Cadence's Integrity 3D-IC platform enables cross-die planning, implementation and multi-die STA, which our research teams demonstrated on a multi-core high-performance design."

***Eric Beyne,** senior fellow and program director, 3D System Integration, imec*

"To push AI acceleration using optical computing, we've consistently leveraged all the latest, innovative trends in the chip design industry—a key innovation being multi-chiplet stacking. In order to build a heterogenous multi-chiplet stacked design, it is important to have a fully integrated planning and implementation system, which can represent multiple technology nodes in a single cockpit. The Cadence Integrity 3D-IC platform provides a unified database solution with implementation and early system-level analysis capabilities, including timing signoff and electrothermal analysis. It helps us deliver next-generation innovation using optical computing for AI acceleration."

***Yichen Shen, PhD,** founder and CEO of Lightelligence Inc.*

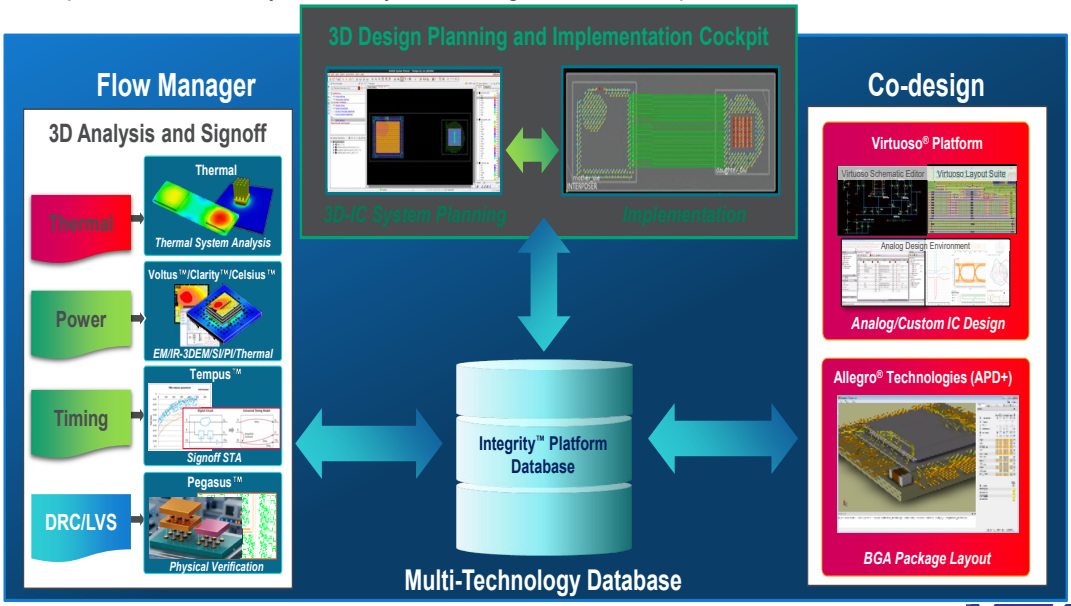
"There are increased requirements for building 2.5D/3D-IC designs with multiple chiplets like logic dies and high-bandwidth memories that are connected with silicon interposer technology. To meet our performance criteria, interposer routing needs automation to be correct-by-construction while taking into account location, shielding and system integrity requirements. The Cadence Integrity 3D-IC platform is well integrated for optimal interposer implementation and system analysis and offers fast, complete system analysis, enabling us to deliver designs that meet memory bandwidth demands for hyperscale computing and 5G communications."

***Tuobei Sun,** R&D head, Department of Packaging and Testing, SaneChips*

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Integrity 3D-IC Platform Overview

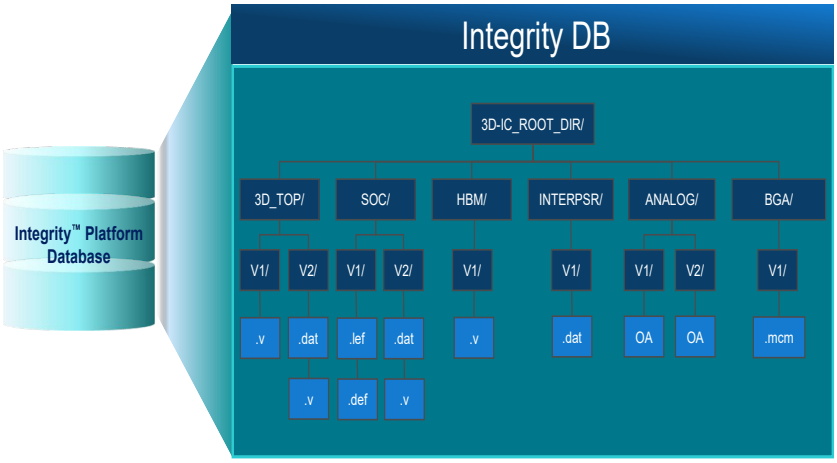
- Industry's first integrated, high-capacity 3D-IC platform that enables 3D design planning, implementation and system analysis in a single, unified cockpit



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Integrity Platform Database

- Database innovation: Can handle multiple technology nodes



- Netlist
- DEF or OpenAccess
- .mcm/.sip
- SDC
- PDK
- MMMC (view definition)
- FlexILM
- ILM
- LEF
- Parasitic
- Metal Fill (physical context)
- SPEF
- Thermal map
- Timing context
- Boundary model
- GDS
- …

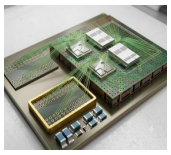
Hierarchical, Multi-Technology, Multi-Level, Multi-Model On-Demand DB

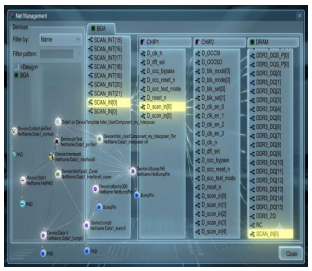
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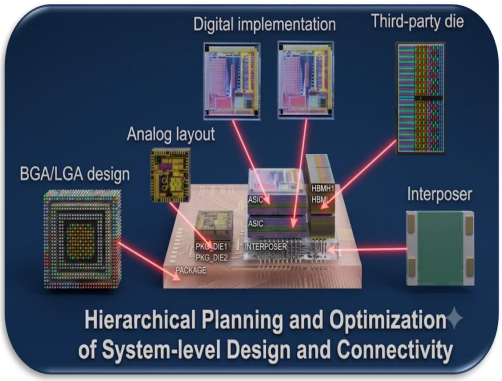
Integrity 3D-IC System Planner

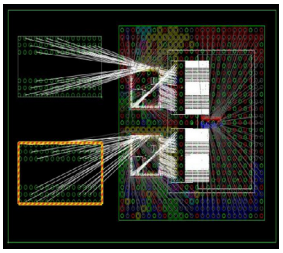
Top-Level 3D-IC Design Management & Optimization



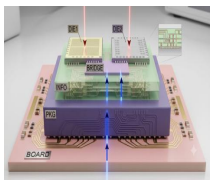


Chip(let)-chip(let)-package-board signal-mapping

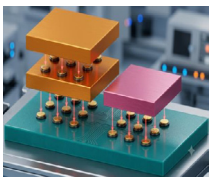




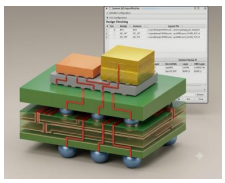
Complete system-level view



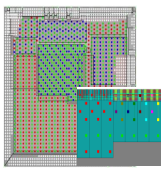
Stack management



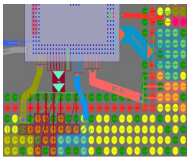
Interface alignment validation



System-level connectivity verification



Advanced bump/TSV planning

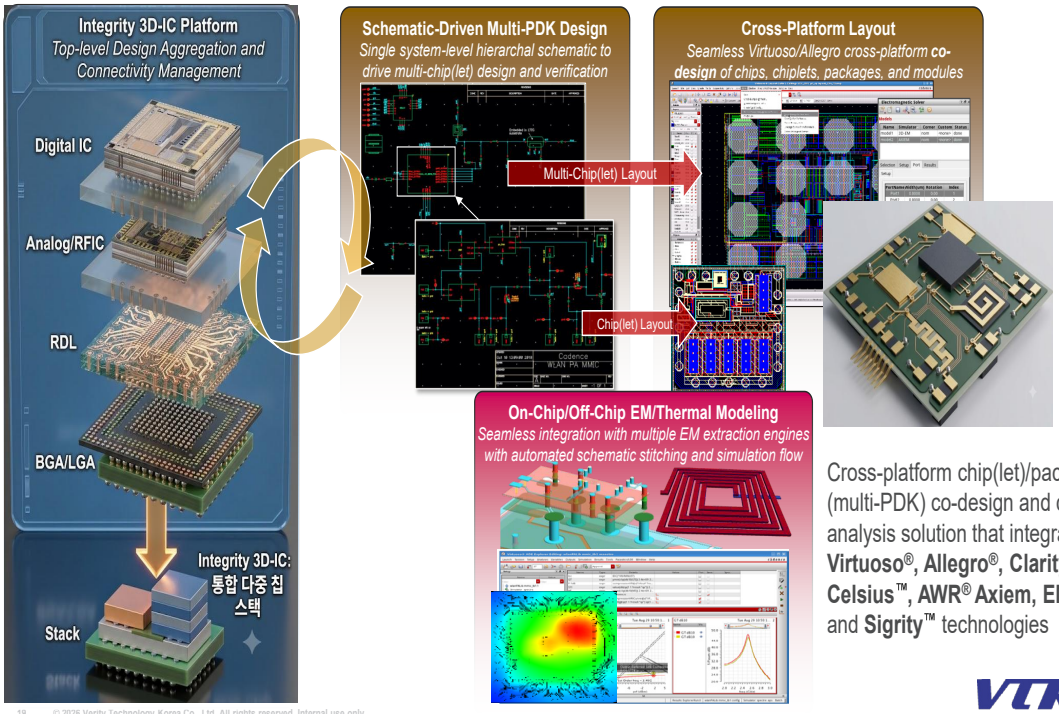


Bundle/bus-driven pin optimization

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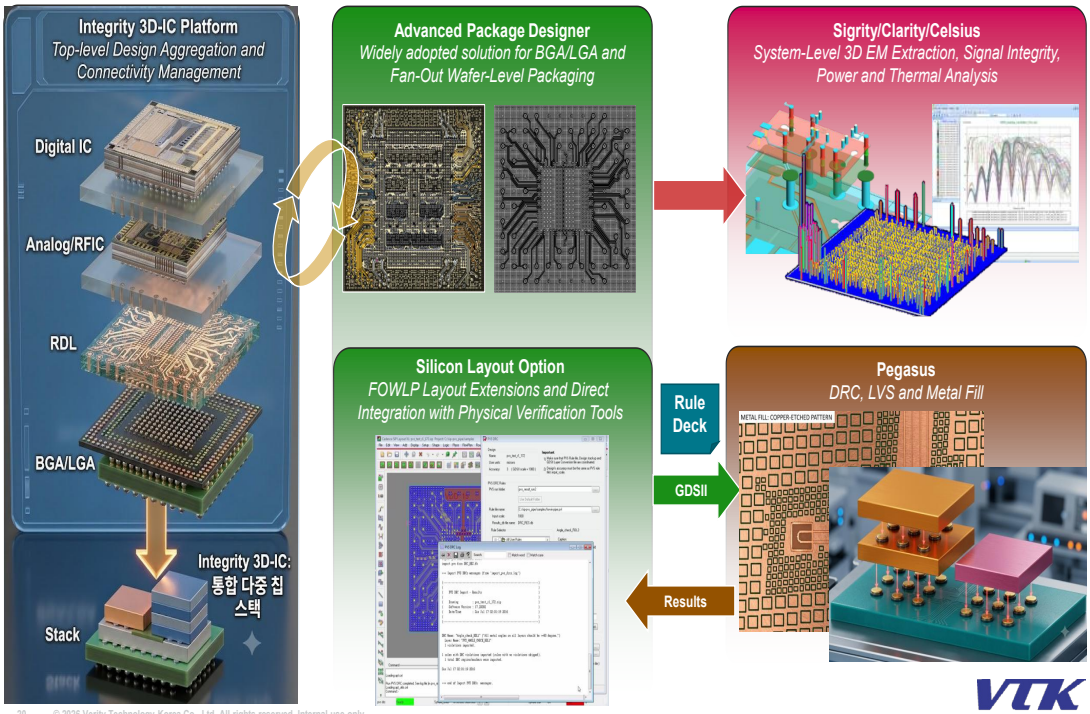
Co-Design with Virtuoso Analog/ RF Multi-Chiplet System-Level Platform



Cross-platform chip(let)/package (multi-PDK) co-design and co-analysis solution that integrates **Virtuoso®**, **Allegro®**, **Clarity™**, **Celsius™**, **AWR® Axiem**, **EMX®**, and **Sigrity™** technologies

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Co-Design with Allegro for BGA/LGA and FOWLP Design



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Integrity 3DIC Co-Design with Virtuoso & Allegro (APD+)

Integrity System Planner

- Bump creation and net assignment for Digital Die
- Bump creation and bump optimization for interposer
- Package creation and net assignment for package balls

Innovus

- Complete digital die implementation,
- Full or partial bump assignment . Interposer routing
- System level ECO's with the planner

Virtuoso

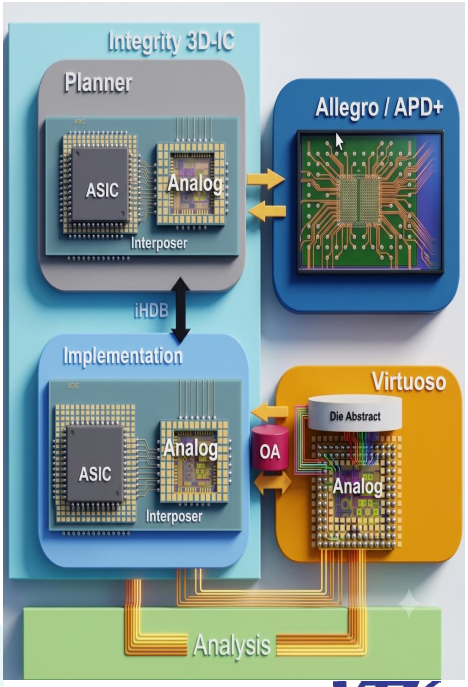
- Complete analog die implementation and bump assignment
- Creation of a die abstract for use by system planner and Innovus

APD+

- Package implementation and Package routing

Enables package implementation along with the die stack

Full system analysis enabled with stack database including package layout

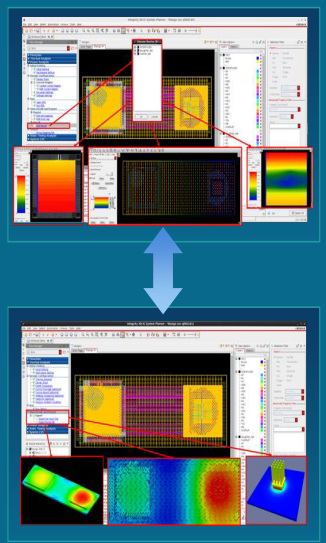


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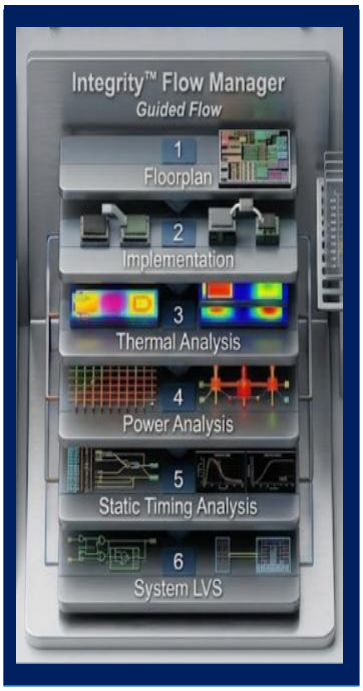
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Integrity 3D-IC Early System-Level Analysis and Signoff Flow

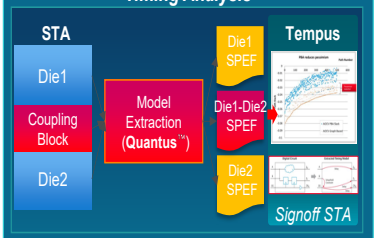
Voltus™/Celsius™
Early Rail (Power and Thermal) Analysis



System-Level Power and Thermal Analysis

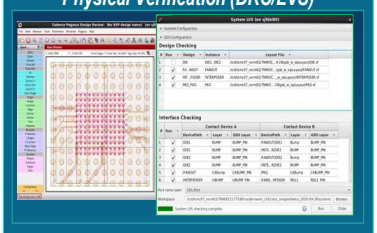


Tempus™
Timing Analysis



3D Analysis with RAID Technology

Pegasus™
Physical Verification (DRC/LVS)



Inter-Die Connectivity Checking

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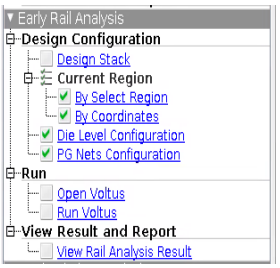
3D-IC Early Rail Analysis – Voltus IC Power Integrity Solution

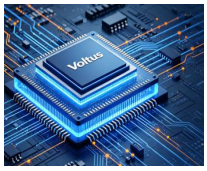
Supports user defined Current Region by selected area or coordinates

Design stacking aware Power Pad Location and multi-die bump mapping table generation automatically.

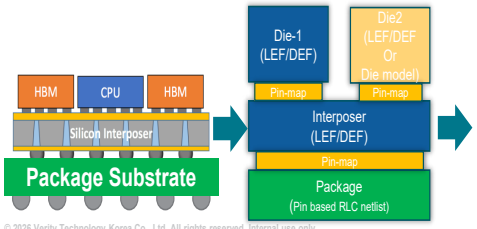
Table-based Die level data configuration.

Die-based ERA result display

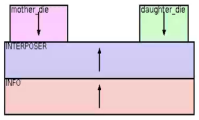


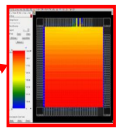


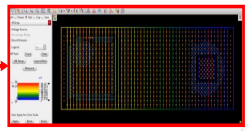
#	Name	Template	Type	Power			
				DEF	PGV Library	QRC Tech File	TSV Subcircuit
1	INFO	INFO	PACKAGE				
2	INTERPOSER	INTERPOSER	DIE	/ic...ef.gz	/icd/t...oser/pgv	/icd/ts...cTechFile	/icd/ts...T/tsv.ckt
3	daughter_...	daughter_die	DIE	/ic...ef.gz	/icd/t..._die/pgv	/icd/ts...cTechFile	
4	mother_die	mother_die	DIE	/ic...ef.gz	/icd/t...gv_macro	/icd/ts...cTechFile	

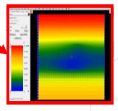








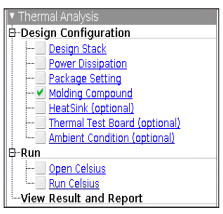


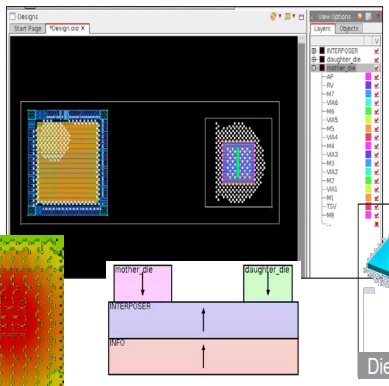


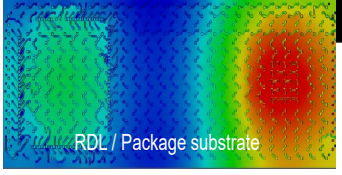
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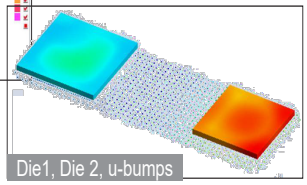
3D-IC Early Thermal Analysis – Celsius Thermal Solver

- Integrates Celsius thermal solver
- Enable early stage Thermal analysis capability
- Multi-die stacking with real Package (.mcm/.sip) and thermal test board
- Guided steps for Bump height, material, underfill, molding compound, heatsink configuration



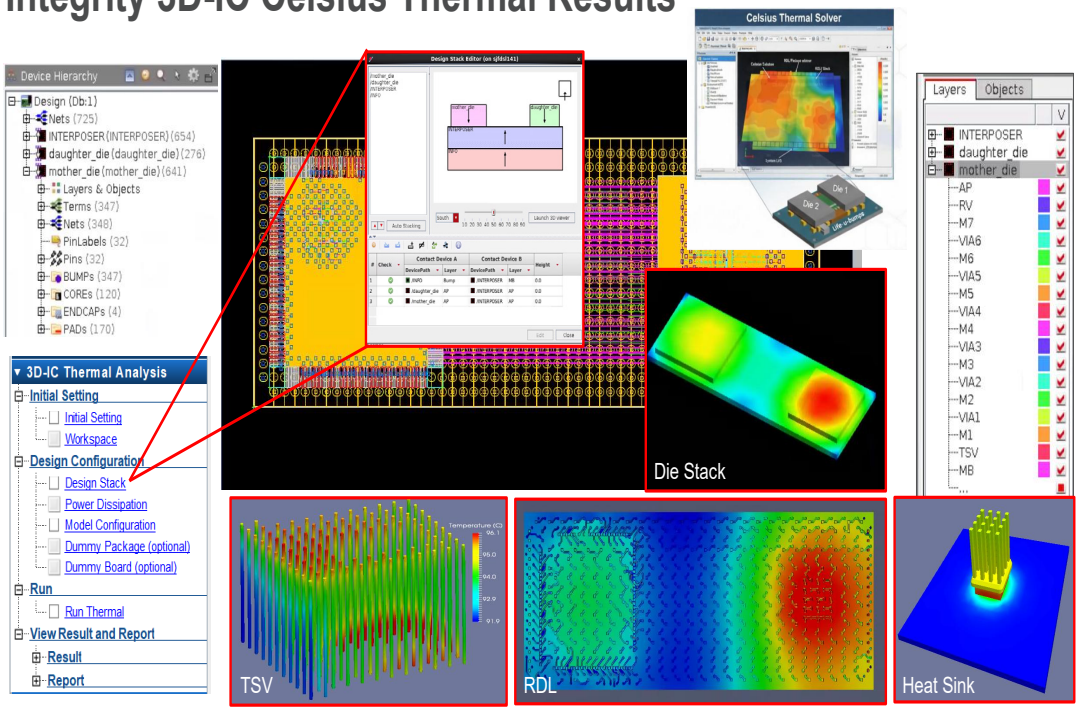






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Integrity 3D-IC Celsius Thermal Results

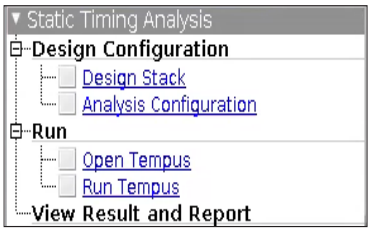


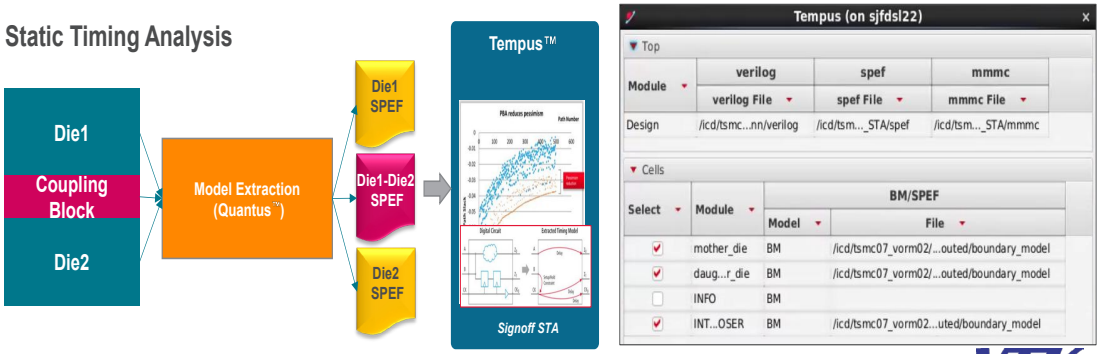
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3D-IC Timing Analysis – Tempus Timing Signoff SolutionStatic

- Integrates Tempus timing signoff engine
- Die-to-die coupling effect consideration
- STA flow with iHDB tag-based input data configuration.
- Offer flexible use models to load-n-Open or Run STA directly.
- Run script template generated for reusing



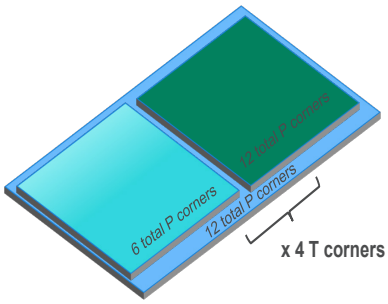


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3D Static Timing Analysis Tempus Technologies

3D-IC Signoff Corner Explosion



3000+ Signoff Corners

10X reduction with Tempus RAID technology

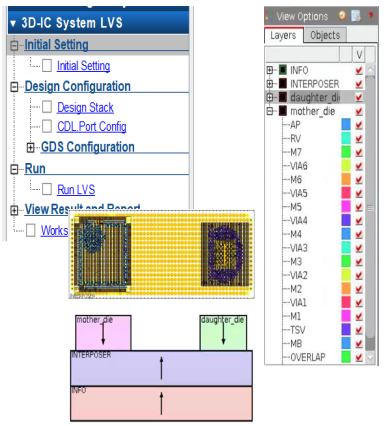
Rapid, Automated Inter-Die analysis (RAID)	• Significantly reduces STA corner data and turnaround time
Concurrent Multi-Mode Multi-Corner (C-MMMC)	• Simplifies job management and machine resources
Boundary Model	• Die-level hierarchical abstract for data reduction
Tempus™ ECO Option	• Concurrent multi-die 3D-IC timing ECO for System-Driven PPA

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3D-IC System LVS (Rule-Deck-Free) - Pegasus Verification System

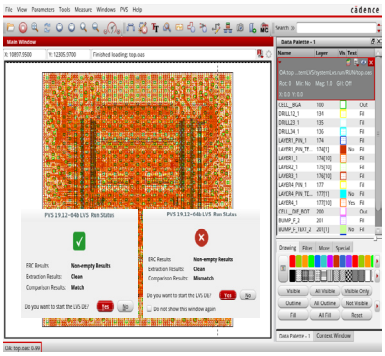
- Integrates Pegasus verification system
- Checks bump alignment/off-set and system-level connectivity using self generated data
- GUI driven interface allows user to define location of GDS, contact layer and design/interface
- Integrated with GDS Viewer for debugging



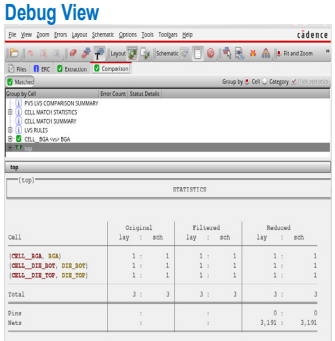
Configuration



GDS View



Debug View

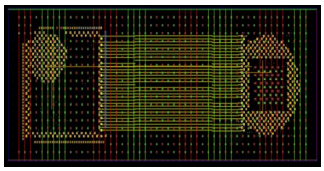


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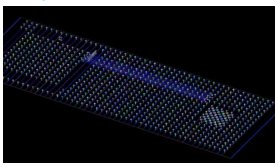
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High-speed IO simulation Flow support

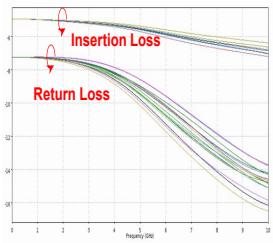
- Clarity 3D FEM to extract S-parameter for high speed IO channel at Interposer



Clarity 3D FEM Extraction

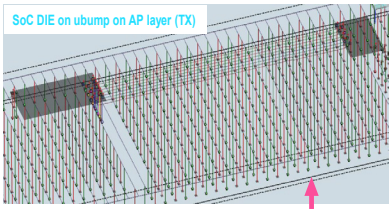


Extracted S Parameter

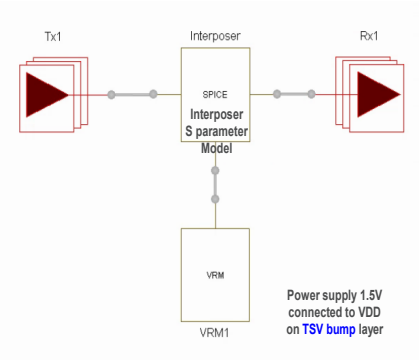


- SystemSI to analyze time-domain eye-diagram simulation

Power and Signals connected to SoC DIE on ubump on AP layer



Power supply on TSV bump layer



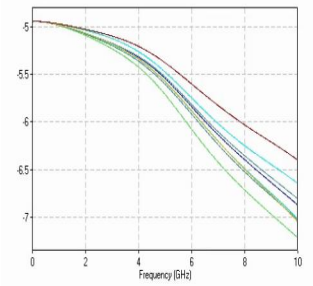
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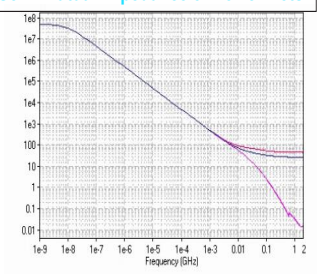
3DIC EM Analysis – System Analysis Using SystemSI

- Time Domain and Frequency Domain Analysis by System SI
- Driven by Cadence Spectre as the circuit engine

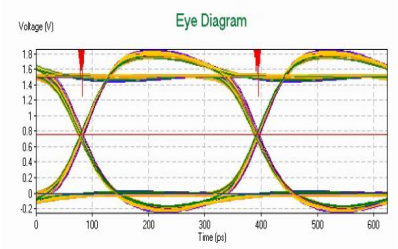
Frequency Domain Analysis – Insertion Loss of Signal Nets



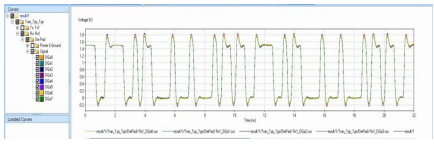
Frequency Domain Analysis – Self / Mutual Impedance of Power Nets



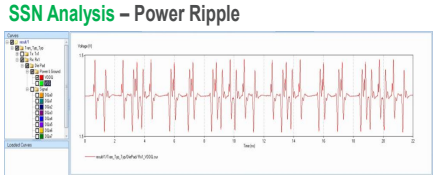
SSN Analysis – Eye diagram with Jitter Histogram



SSN Analysis – Signal Waveform



SSN Analysis – Power Ripple



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